Real-Life Mission Profile-Oriented Lifetime Estimation of a SiC Interleaved Bidirectional HV DC/DC Converter for Electric Vehicle Drivetrains

Chakraborty, Sajib ; Hasan, Mohammed Mahedi ; McGahan, Paul; Tran, Dai-Duong; Geury, Thomas ; Davari, Pooya; Blaabjerg, Frede; El Baghdadi, Mohamed ; Hegazy, Omar

Published in:
I E E E Journal of Emerging and Selected Topics in Power Electronics

DOI (link to publication from Publisher):
10.1109/JESTPE.2021.3083198

Publication date:
2022

Document Version
Accepted author manuscript, peer reviewed version

Real-Life Mission Profile Oriented Lifetime Estimation of a SiC Interleaved Bidirectional HV DC/DC Converter for Electric Vehicle Drivetrains

Sajib Chakraborty, *Member, IEEE,* Mohammed Mahedi Hasan, McGahan Paul, Dai Duong Tran, *Member, IEEE,* Thomas Geury, Pooya Davari, *Senior Member, IEEE,* Frede Blaabjerg, *Fellow, IEEE,* Mohamed El Baghdadi, *Member, IEEE* and Omar Hegazy, *Member, IEEE*

***Abstract*— The rapid growth of Battery Electric Vehicles (BEVs) in the automotive field has led to a need for improving their drivetrain performance, mainly focusing on the extension of the battery operating range. However, the majority of performed technical assessments only consider battery SoC and depth of discharge while neglecting the effects on lifetime and failure probability of power electronic components, more specifically the emerging wide-bandgap-based (WBG) technologies. Toward fulfilling this gap, the EV market demands lifetime estimation performed under real-life mission profile to confirm efficiency and reliable operation of EV power electronics for an extended range meeting the EVs lifetime requirements. In this regard, the present study proposes a versatile experimental device-under-test setup to investigate a novel stepwise holistic system-level lifetime estimation approach for BEV drivetrains equipped with SiC interleaved bidirectional HV DC/DC converter (IBC). To this end, three different real-life mission profile use-cases are investigated in this paper and provides systematic stress-based lifetime estimation, statistical analyses, and validations in comparison. The study outcome highlights realistic information related to significant impacts of operation range and battery SoC features on the IBC lifetime from all aspects.**

***Index Terms*—Real-life mission profile, power electronics reliability, battery pack SoC, interleaved DC/DC converter, SiC power modules, Electric Vehicles, Monte Carlo optimization, Weibull fit, component-level lifetime, system-level lifetime.**

I. Introduction

Battery Electric vehicles (BEVs) are rapidly gaining popularity and are expected to achieve a 30% market share in all modes of automotive industries by 2030 [1]. The main concerns regarding widespread adoption of the EVs are comfort, range, safety, battery lifespan, fast charging, control robustness and ageing [2]. Regarding the latter, the standards *AEC Q100, Q101, Q200* are used as stress/lifetime testing qualification in the automotive industry [3]. Hence, the power electronics converters (PECs) mounted on BEVs need to satisfy the automotive lifetime requirements [4]. Moreover, failure of the EV's PECs accelerates the unplanned maintenance cost up to 59% [5]. It is found from field test data that the PECs are responsible for 37% of the unscheduled maintenances in the electrical traction systems [5]. Therefore, in BEVs, the lifetime estimation of the PECs draws the attention of both academia and automotive original equipment manufacturers (OEMs). An industry-oriented survey of eighty companies [6] mentioned that semiconductor devices are the most failure-prone components and responsible for overall 31% of the failures in the PECs.

A. The necessity to investigate SiC power module's failures

As this paper is focused only on SiC-based technology, the SiC power module failures need to be investigated thoroughly. There are two fundamental modes for SiC power modules: (a) *wear-out failures* and (b) *catastrophic failures*, as mentioned in [7], [8]. Packaging failures constitute wear-out failures, where the failure is a consequence of accumulated damage due to the temperature, threshold voltage, vibration, and humidity stresses on the SiC power module. Within these stress factors, the temperature, or more precisely, the junction temperature, is considered the most critical in inducing failures in the SiC power modules. The cross-sectional view of a SiC MOSFET module is depicted in Fig. 1, which represents different types of possible wear-out damage due to varying coefficients of thermal expansion (CTE) among the various materials in a wire-bonded SiC power module package [7],[9].

According to the accelerated lifetime testing (ALT) of the SiC power modules, as mentioned in [10]–[15], due to the CTE mismatch between the adjacent layers, the bond wire and die attach-solder layer is identified as the most vulnerable area. Moreover, the thermo-mechanical stresses coming from temperature swings in these two areas accelerate the degradation, leading to various wear-out damages such as bond wire hill-crack, bond wire lift-off and solder joint damage. In addition to that, the extreme mean junction temperature in the SiC power module is responsible for bond wire-body and chip metallization damages. On the contrary, the SiC power module's catastrophic failures occur when the operating conditions exceed the limits of the SiC properties of critical breakdown electric field (MV/cm) and thermal conductivity (W/cm/K). Overheating, overvoltage, or overcurrent operating conditions can activate such catastrophic failures.

SiC power modules also suffer from steady-state attrition over the long term due to intrinsic wear out. One such failure is the time-dependent dielectric breakdown (TDDB), a kind of ageing that MOSFETs suffer from due to the breakdown of the gate oxide that occurs as a result of the application of gate voltage [16], [17]. Such failures can cause ageing issues for power modules that last in the long term.

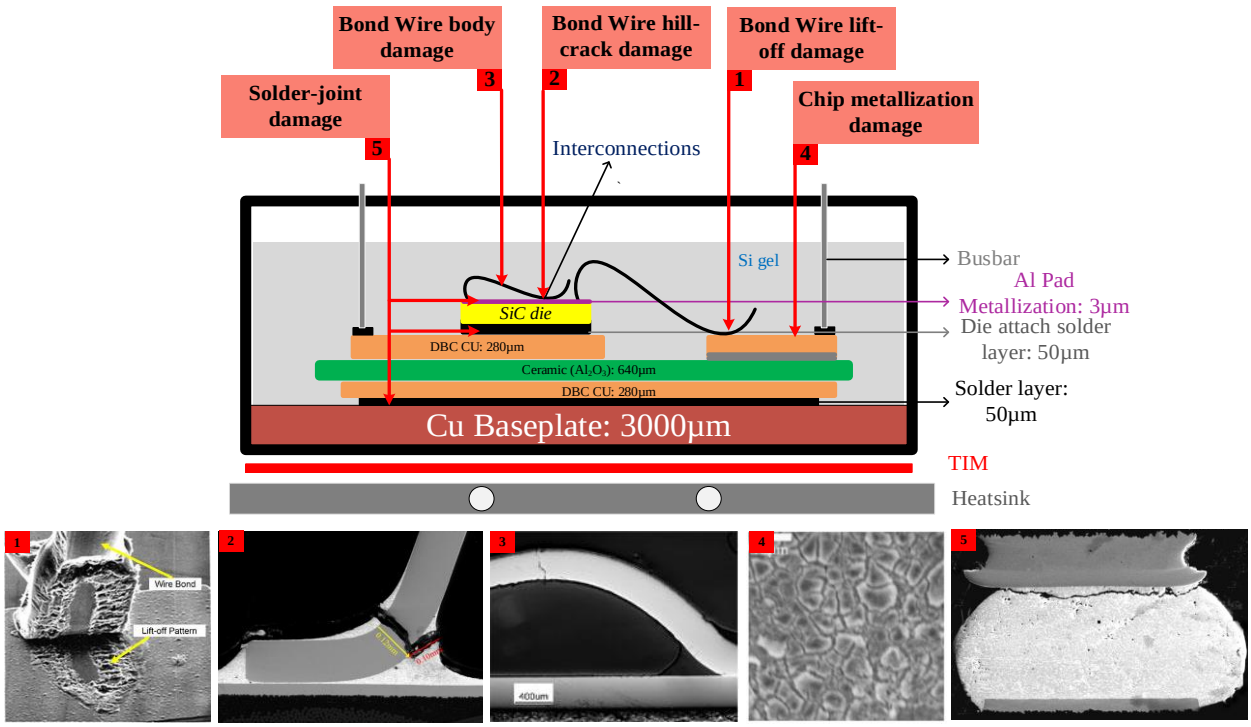


Fig. 1. Cross-sectional schematic of a SiC power module with the coefficient of thermal expansion, here scanning electron microscopy (SEM) images of the following failure mechanisms are illustrated: (1) bond wire lift-off damage [18], (2) bond wire hill-crack damage [19], (3) bond wire-body damage [19], (4) chip metallization damage [18] and (5) solder-joint damage [20]. The potential failure positions in the SiC MOSFET power module is also indicated via red arrow.

Such failure can also occur due to extrinsic or intrinsic reasons; since extrinsic factors, such as manufacturing defects, are weeded out through qualification testing, this research considers the intrinsic factors, like electrical stress, which could cause wear out. Hence, this research study is focused on investigating the SiC power module's wear out due to electro-thermal stress and the intrinsic effects of dielectric breakdown while PECs are in operation and on assessing the failure that might arise through ageing and the TDDB analysis.

B. The necessity to investigate failure caused in the DC-link capacitor

According to the aforementioned industrial survey [6], the second failure-prone device in the PEC is the DC-link capacitor. The DC-link capacitor is responsible for the root cause of 19% of all failures. On the one hand, the electrolytic DC-link capacitor's cost-effectiveness and simplicity make it a preferable choice for the PECs developers [21]. On the other hand, the electrolytic DC-link capacitor can give rise to ageing issues. The potential cause of electrolytic DC-link capacitor ageing is the uneven electro-thermal reaction and/or electrolytic evaporation. These ageing factors are accelerated due to excessive electro-thermal stresses on the capacitor [21], [22]. The electro-thermal stresses can be increased due to high ripple current and DC-link voltage variation. The ripple current is responsible for increasing the Equivalent Series Resistance (ESR) over time, hence, increasing the hot spot temperature to accelerate the ageing impact on the electrolytic DC-link capacitor. Therefore, in this paper, the DC-link capacitor ageing is also investigated for PECs in full load operation.

C. Lifetime requirement of automotive-grade power electronics converters

The BEV lifetime requirement is determined based on the standard set up by automotive OEMs [23]. Currently, BEVs exponentially penetrate the vehicle industry; hence, the automotive PECs are required to be compliant with the standard certification requirements set by *AEC Q100, Q101 and/or Q200* to prevent undesirable failures of the BEVs [3]. The lifetime requirements of commercial light-duty BEVs concerning different scenarios are depicted in Table 1.

The operational lifetime requirement for both traction Inverter and DC/DC converter is 300,000 km/15 years, which assumes around 8000 h operation with an average speed of 37.5 km/h [23]. The lifetime requirement for vehicle-to-grid (V2G) components is 300,000 km/15 years [23]. In contrast, in the integrated BEVs, the lifetime requirement is anticipated to prolong by a factor of 2 (600,000 km) as both the inverter and DC/DC converter usage is doubled [24]. In the future, for shared mobility EVs, the lifetime requirement will be extended to around 2-5 times (600,000 km-1000,000 km) based on autonomous driving and ride-sharing opportunities [25].

TABLE 1. BEV'S LIFETIME REQUIREMENTS REGARDING SCENARIOS.

Scenario 1: Standard EVs	**Scenario 2: Vehicle to Grid Applications**
Traction Inverter (300,000 km/15 years) DC-DC converter (300,000 km/15 years)	Traction Inverter (300,000 km /15 years) DC-DC converter (300,000 km /15 years)
Scenario 3: Integrated PE System	**Scenario 4: Sharing Vehicles**
Traction Inverter (600,000 km/15 years) ~2 times DC-DC converter (600,000 km/15 years) ~2 times	Traction Inverter (600,000/1000,000 km) ~ (2-5) times DC-DC converter (600,000/1000,000 km) ~ (2-5) times

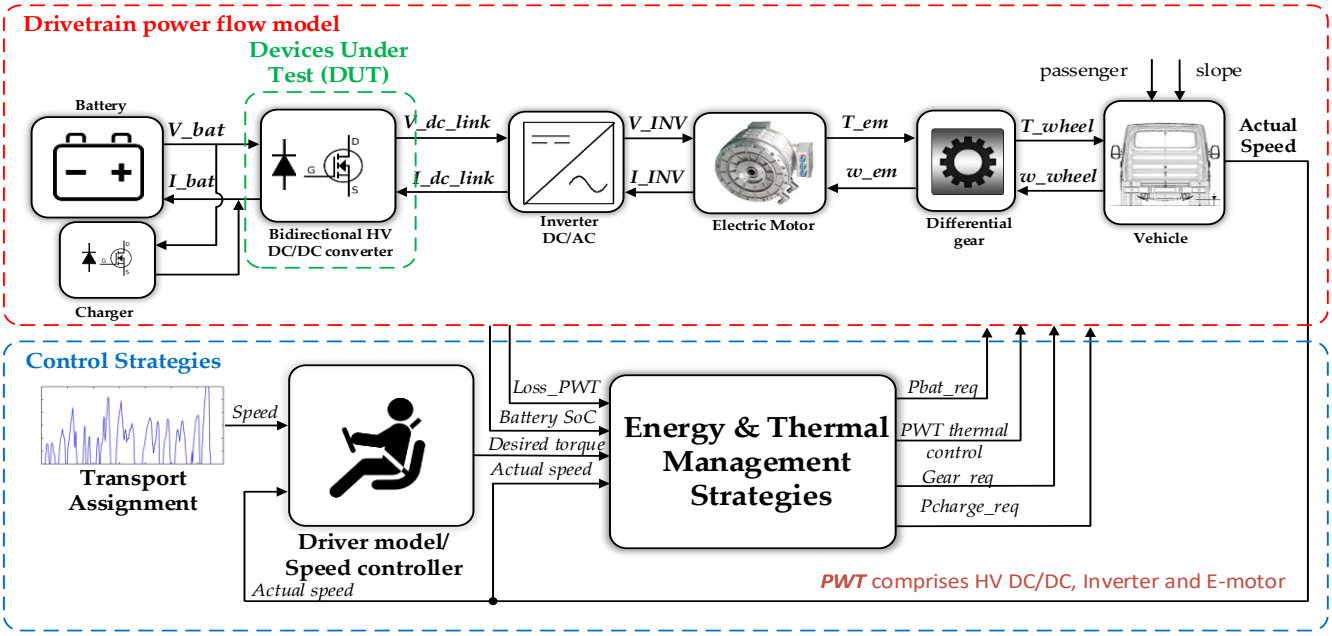


Fig. 2. Bidirectional HV DC/DC converter in an EV-drivetrain application along with EMS and TMS strategies.

D. Role of HV DC/DC converter in E-drivetrain

Fig. 2 illustrates simplified vehicle architecture, which comprises of a battery pack, bidirectional HV DC/DC, inverter, electric motor (EM), differential transmission and rear-wheel drive, and is also considered as a baseline vehicle for this research study [26]. In BEV powertrain architecture, the addition of an HV DC/DC converter can have several benefits. First of all, booster mode allows higher and variable DC-link voltage operation, which offers 1.5% lower losses in the drivetrain components (i.e., improvement of losses in inverter by 37.6% and motor by 5.4%) and improves the battery pack ageing [26], [27]. Due to the HV DC/DC converter, system design dependency on the customer's battery pack voltage is reduced, which improves the design scalability [26]. The inclusion of the HV DC/DC converter can reduce the number of series cells and significantly reduce the EV battery pack cost, which has a considerable impact on the overall EV system cost. Besides, the HV DC/DC converter improves the efficiency of regenerative braking and reduces the DC-link capacitance size. The HV DC/DC converter has a number of shortcomings, primarily costs and losses of the converter itself. These disadvantages can be considered as a trade-off.

E. Lifetime research trends of automotive power electronics converter

The lifetime of a bidirectional DC/DC boost converter in Series-Hybrid EVs (SHEV) is described in [28]. FTP-75 was used as a mission profile, while the initial battery SoC was considered 100%. A multistate Markov analysis in lifetime evaluation for interleaved DC/DC converter is presented in [29]. A MILHDBK-27F based lifetime estimation was utilized in that research. A MILHDBK based parts count method was being used for the lifetime estimation of a bidirectional HV DC/DC converter in a hybrid electric vehicle (HEVs) [30]. The lifetime of possible bidirectional DC/DC converter topologies for an efficient EV is studied in [31]. Failure in time (FIT) rates were calculated for lifetime calculation of the HV DC/DC converters based on a 30-minute generic drive cycle with less dynamics behaviour.

A mission-profile-oriented lifetime prediction of the PECs for a series-HEV (Toyota Prius) is shown in [32], where the initial battery SoC was considered 100%. The reliability coefficients were used based on the reliability book RDF 2000. The extra-urban driving cycle (EUDC) based lifetime estimation of the used PECs applied in the EVs is studied in [3]. An empirical model was utilized to estimate the PEC lifetime in the ppm range (0.001%). A systematic approach for lifetime evaluation of the DC converter in DC microgrid system is analysed in [33], where high initial state-of-charge (SoC) of the battery, mission profile, and dynamic load variations were studied.

The main shortcoming of these studies is the mission profile formulation utilized in the lifetime estimation process. These studies used only standard driving cycles as NEDC, WLTC, FTP-75 and EUDC. Previous research in [3], [28]-[32], had not considered real-life mission-profile measurements. The device-level loading factors of the PECs are highly dependent on the mission profile, which significantly impact the ageing of the device under test (i.e., PECs). Moreover, the actual battery pack responses based on the real-life mission profiles have remained unimpeded so far in the literature.

F. The main contribution of this research paper

In this paper, three distinct real-life mission profiles have been utilized as the EV loading factors with separate initial battery pack SoC (i.e., *95%*, *75%*, *35%*), while previous research in [3], [28]-[32] applied standard mission profile, high SoC range of batteries and/or generic EV parameters. Some of these publications did not consider the battery and its associated SoC conditions [3], [29]-[31]. However, it is well known that battery pack behaviour can vary significantly from high SoC to low SoC (i.e., battery voltage, current and temperature) [34].

Previous research in [3], [28]-[32] considered a constant coolant temperature response (60^{O}C), while the impact of the powertrain thermal systems (PWTs) had not been applied.

However, according to [3], [35]–[37], the long-term reliability of the PECs is highly dependent on the active temperature cycling, which is basically generated through the PWTs. PWTs behaviour dynamically varies based on the driving profiles, environmental temperature and heat generated from the PECs. The PWTs may impose higher stress on the PECs; therefore, thermal cycles caused by the PWTs are considered as stress loading factors. In this paper, the inlet coolant temperature of the PWTs has been used as an active cyclic thermal stressor.

Nowadays, it is of high importance for automotive OEMs to guarantee the reliable operation of the PECs to avoid unexpected downtime of the entire EV system and therefore reducing warranty costs. Hence, failures in the PECs need to be tracked and resolved using highly accurate and dependable lifetime estimation processes; in most cases, it is not possible due to the unavailability of base vehicle modelling parameters. Hence, in this paper, the real-life EV mission profile-oriented physics-of-failure (Pof) based lifetime method has been utilised to accurately assess the PEC lifetime based on the parameters of the baseline vehicle and measurement data.

Ageing research carried out in [3], [28]-[32], assessed the lifetime of Silicon-based PEC, while in this paper, the Pof-based lifetime estimation method of Silicon Carbide (SiC)-MOSFETs based PEC through a highly accurate electro-thermal model has been investigated.

This paper also proposes a stepwise holistic framework for real-life mission profile-oriented lifetime estimation of a SiC-based HV DC/DC converter for the EV applications to fill the above-mentioned research gap. This paper estimates the system-level lifetime based on separate real-life mission profiles from the real EV measurement; in this research study, different initial battery SoC and RMS C-rate are considered. Besides, dynamic inlet coolant temperature profiles are considered for the converter. All these crucial dynamic factors are not fully addressed in previous studies. Hence, this article performs a system-level lifetime estimation considering the impact of real-life mission profiles and device-level loading factors on the component-level lifetime (i.e., SiC-based power devices and DC-link capacitors).

G. Paper structure

The rest of the article is organized as follows. In Section II, the baseline vehicle from where the real-time (RT) test data are measured is described in detail. The detailed mission profiles and device-level loading factors, description of battery pack modelling and validation, powertrain thermal system modelling approach, HV DC/DC converter control system, the electro-thermal modelling and validation are given in Section II. In Section III, stepwise real-life mission profile-oriented lifetime estimation method of an automotive HV DC/DC converter is presented at component-level. Afterwards Section IV is carried out the lifetime evaluation of the HV DC/DC converter for three mission-profiles. In Section V, the intrinsic effect on the power modules has been added with the reliability obtained using Monte-Carlo simulation with parametric variation that leads to a full assessment of the system-level lifetime both with and without redundancy. Finally, concluding comments of the presented work and guidelines for future lifetime estimation research are discussed in Section VI.

II. EV MODELLING & LOADING FACTORS ANALYSIS

A. Parameterized battery electric vehicle modelling

In this paper, a utility BEV drivetrain system has been modelled in MATLAB/Simulink® using a forward-facing approach [26], [38]–[40]. The simulation model is required to evaluate the vehicle performance, such as vehicle speed, battery SoC, electrical energy over a specific driving cycle. The BEVs drivetrain consists of a driver model, EM, inverter, HV DC/DC converter, transmission, gearbox, vehicle dynamic model, environment model, energy storage system (ESS), the energy management system (EMS) and thermal management system (TMS). Each component can be calibrated in standalone mode with a semi-automatic calibration approach based on the least-squares method. Low-fidelity (LoFi) efficiency map-based inverter and EM model are utilized, whereas a constant efficiency is used for the gearbox losses estimation and final drive transmission. The energetic vehicle model based on the longitudinal dynamic motion laws is developed.

The measured mission profiles provided by OEM are fed into the driver model, which generates the total requested torque at the wheels and brake commands. The torque command goes into the EM model, while the brake command first goes into the vehicle dynamics model. Afterward, the torque is translated into speed, with the required power that is provided through the ESS. Component by component, this power flow is propagated through the drivetrain, considering losses. The EMS supervises the entire process and ensures that the flow of energy within the BEV drivetrain is optimal. The TMS provides setpoints to the powertrain thermal system. A parameterized radiator-fan-based cooling circuit is used to safely dissipate heat generated from the powertrain (HV DC/DC, inverter, and EM) while maintaining the junction temperature of the HV DC/DC converter below 145^0C. Based on the initial battery SoC the battery pack voltage varies from 250 V-320 V. The DC-link voltage is maintained at a constant 400 V, and bi-directional energy transfer is performed using the HV DC/DC converter. The detailed baseline vehicle modelling parameters are shown in Table 2.

TABLE 2. EV MODELLING PARAMETERS.

Description	Unit	Values
Gross vehicle weight	*kg*	3600
Vehicle glider weight	*kg*	1213
Battery	*kg*	200
Inverter & HV DC/DC converter	*kg*	25
Motor	*kg*	16.8
Gearbox	*kg*	30
HV Wiring	*kg*	30
Kerb weight (unladen mass)	*kg*	1504.8
Driver + equipment according WLTP regs	*kg*	100
Mass in running order	*kg*	1604.8
Gearbox ratio (motor to wheel)	*[-]*	9.3: 1
Gearbox efficiency (motor to wheel)	*[%]*	0.98
Tyre size for comparison	*[-]*	195/75 R16
Rolling Resistance Coefficient (RRC)	*[-]*	0.00769
Drag coefficient (Cd)	*[-]*	0.52
Frontal Area	m^2	4.284
Power net load	*W*	450
Nominal Electric Motor power	*[-]*	60kW
Battery cell-chemistry	*[-]*	NMC
Series and parallel string	*[-]*	18S,4P
Nominal Energy	*kWh*	19.5
Nominal Voltage	*V*	320

TABLE 3. EV MISSION PROFILE CHARACTERISTICS, INITIAL BATTERY CONDITIONS AND ENVIRONMENTAL SCENARIOS.

Speed Profile	Environmental scenarios	Battery condition	Characteristics
Extra-Urban Cycle	Negligible traffic condition, medium-high slopes, Vehicle load = 3200 kg and Ambient temperature 40°C.	Initial SoC 95%, Final SOC 60% and RMS C-rate of 0.5 C	Distance:20.6 km, Duration: 4845 s Average speed: 4.24 m/s Maximum acceleration: 8.68 ms^{-2} Minimum acceleration: -8.85 ms^{-2}
Urban Cycle	Negligible traffic condition, medium-high slopes, Vehicle load = 3200 kg and Ambient temperature 40°C.	Initial SoC 75%, final SOC 30% and RMS C-rate of 1.5 C	Distance: 20.3 km, Duration: 1500 s Average speed: 13.55 m/s Maximum acceleration: 1.87 ms^{-2} Minimum acceleration: -2.25 ms^{-2}
Continuous hill-climbing Cycle	Constant power, high slopes, Vehicle load = 3200 kg and Ambient temperature 40°C.	Initial SoC 35%, final SOC 20% and RMS C-rate of 1.5 C	Distance: 2.3 km, Duration: 160 s Average speed: 13.77 m/s Maximum acceleration: 19.03 ms^{-2} Maximum acceleration: -19.33 ms^{-2}

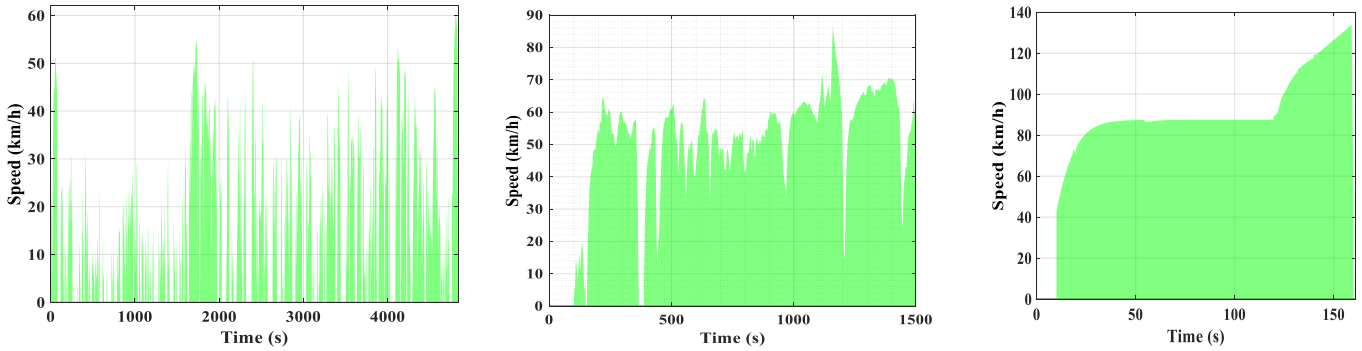


Fig. 3. Mission profiles: (a) extra-urban 4845 s long, (b) urban 1500 s long and (c) continuous discharge 160 s long at same environmental condition.

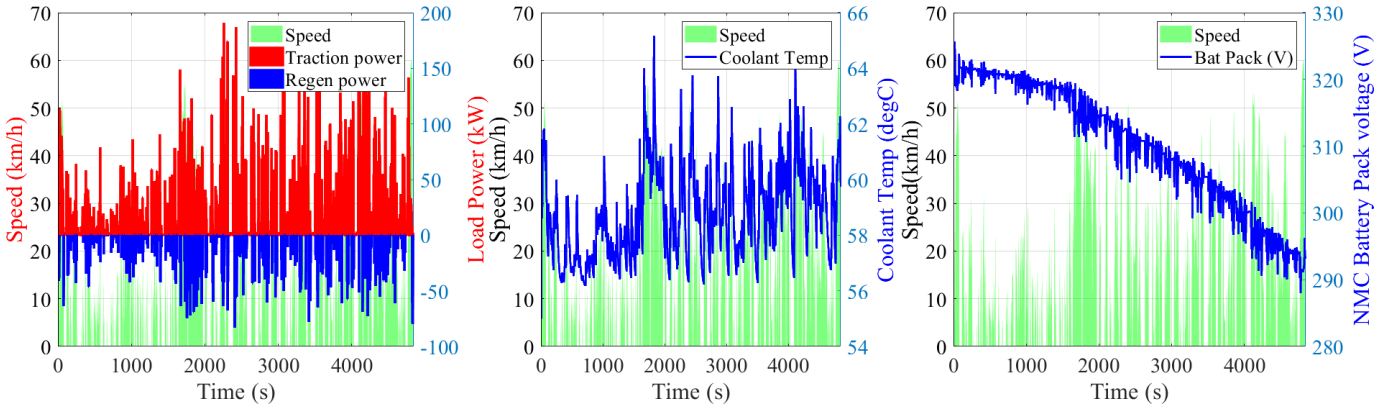


Fig. 4. Load profiles of the automotive IBC during extra-urban mission profile.

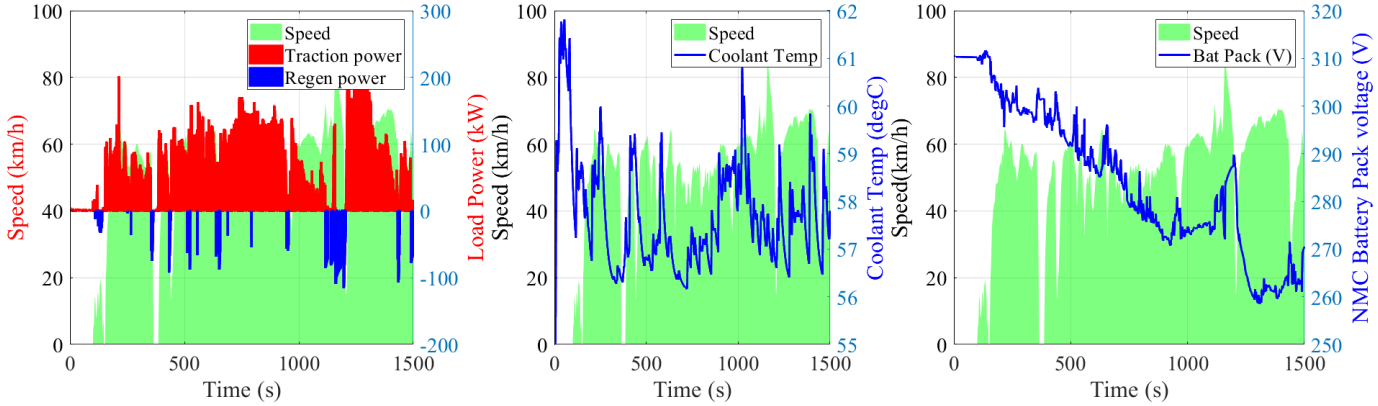


Fig. 5. Load profiles of the automotive IBC during urban mission profile.

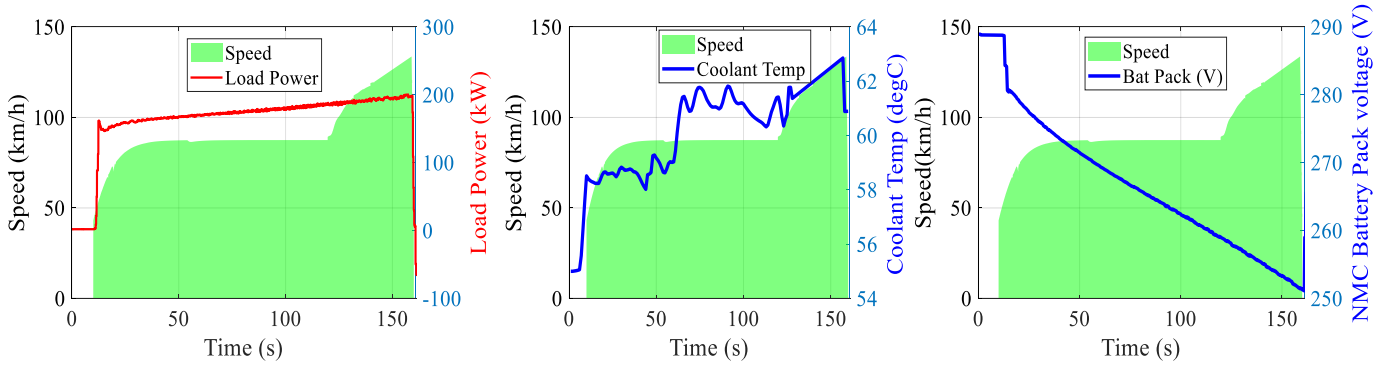


Fig. 6. Load profiles of the automotive IBC during Continuous hill-climbing mission profile.

B. EV mission profiles and device loading factors for case study

In this paper, three mission profiles are received from the real-life chassis measurement of an OEM. These mission profiles are categorized into three types of cycle sections, as shown in Table 3. These three cycles were developed for consumption testing of a specific BEV. Furthermore, specific BEV parameters are used for the dynamic modelling of the entire BEV, as mentioned in the previous sub-section. Several environmental conditions (i.e., traffic conditions, vehicle load and the ambient temperature) were kept constant during the measurement as the same stretch of the road is used to generate distinct mission profile. The changes were performed in the initial battery condition (i.e., initial SoC, voltage and RMS C-rate), as illustrated in Table 3.Moreover, real-life measurements of the battery pack are utilized to validate the LoFi battery pack model used in this paper. The three speed profiles are depicted in Fig. 3, and their characteristics are also presented in Table 3.

The three speed profiles are given as input to the forward BEV model. Based on these mission profiles, device-level loading factors of the HV DC/DC converter are determined. The device-level loading factors consist of the load power demand from the traction inverter (P_{Load}), the dynamic battery pack voltage response (V_{BAT}) and the inlet coolant temperature variation of the powertrain thermal unit ($T_{coolant}$). The dynamic load power response can be obtained from the traction inverter power demand. For the battery pack voltage response, an accurate low fidelity battery pack model using a lumped thermal mass is designed and validated with real-time (RT) measurement, as discussed in sub-section C. Finally, a parameterized radiator fan-based powertrain thermal system is designed to obtain the coolant temperature response, which corresponds to the specific baseline vehicle, as discussed in sub-section D. The device-level loading factors of the HV DC/DC converter during different mission profiles are illustrated in Fig. 4-Fig. 6.

C. Battery Pack modelling and validation

The battery pack under consideration contains 15 Ah pouch cells arranged in 5 series-connected modules. Each module configuration is 4p18s. The pack has a nominal voltage of 320 V and nominal energy of 19.5 kWh. The battery pack modelling approach is presented schematically in Fig. 7 where a complex coupling between electrical and thermal/hydraulic domains via a heat release model is shown.

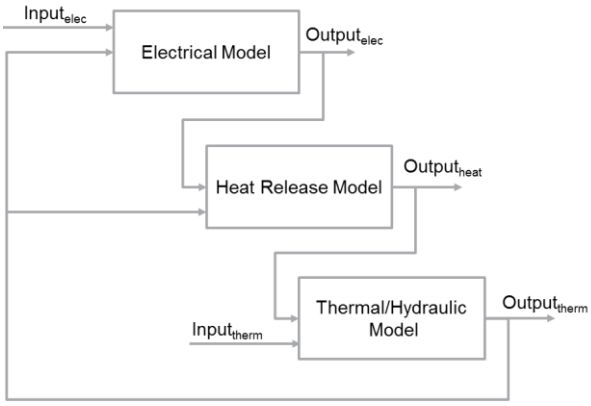


Fig. 7. Battery Pack model schematic.

The system inputs are spread across both electrical (load current) and thermal/hydraulic (coolant temperature, pressure, and flow rate). To model the electrical behaviour of the cell, an Equivalent Circuit Model (ECM) has been used, including parameterisation of internal resistance *Ri*, and one *RC* stage that accounts for polarization effects in the cell. An SoC-controlled voltage source represents the open-circuit voltage (OCV) of the cell. This model is presented schematically in Fig. 8.

The low fidelity model assumes two lumped thermal mass for core and surface of the cell and thermal mass at the top and bottom cooling plate as shown in Fig. 9. The equivalent heat capacitance of the core is denoted by C_c^{modu}, the surface by C_s^{modu} and the cooling plate by C_p^{modu}. The core, surface, top and bottom cooling plate temperatures are denoted by T^c, T^s, T_T^p and T_B^p respectively. The model assumes thermal resistance between core to the surface, denoted by R_{cs}^{modu} and surface to cooling plate, denoted by R_{sp}^{modu}. The surface and cooling plate also have a thermal resistance to ambient denoted by R_{sa}^{modu}, R_{Ta} and R_{Ba} respectively.

The battery pack model has been validated against the RT measurement of battery pack voltage. The RT-measurement of the battery pack voltage has been taken via a CAN Bus module from the chassis of the vehicle. Kendall's rank correlation is utilized for battery pack validation. The formulation of Kendall's rank correlation is provided in the Appendix. The battery pack terminal voltage and SoC validation against RT-test data at three different mission profiles are presented in Fig. 10-Fig. 12.

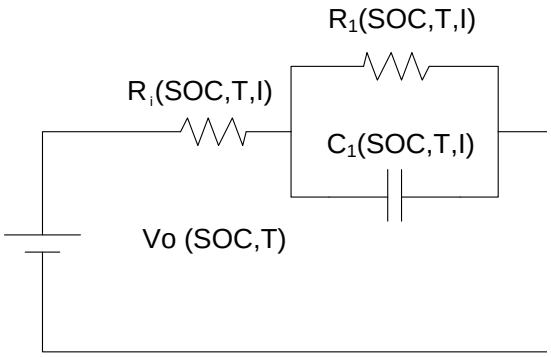


Fig. 8. Electrical 1st order equivalent circuit model schematic of a battery cell.

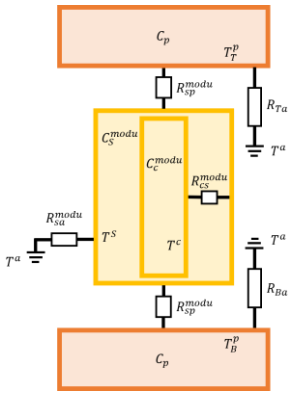
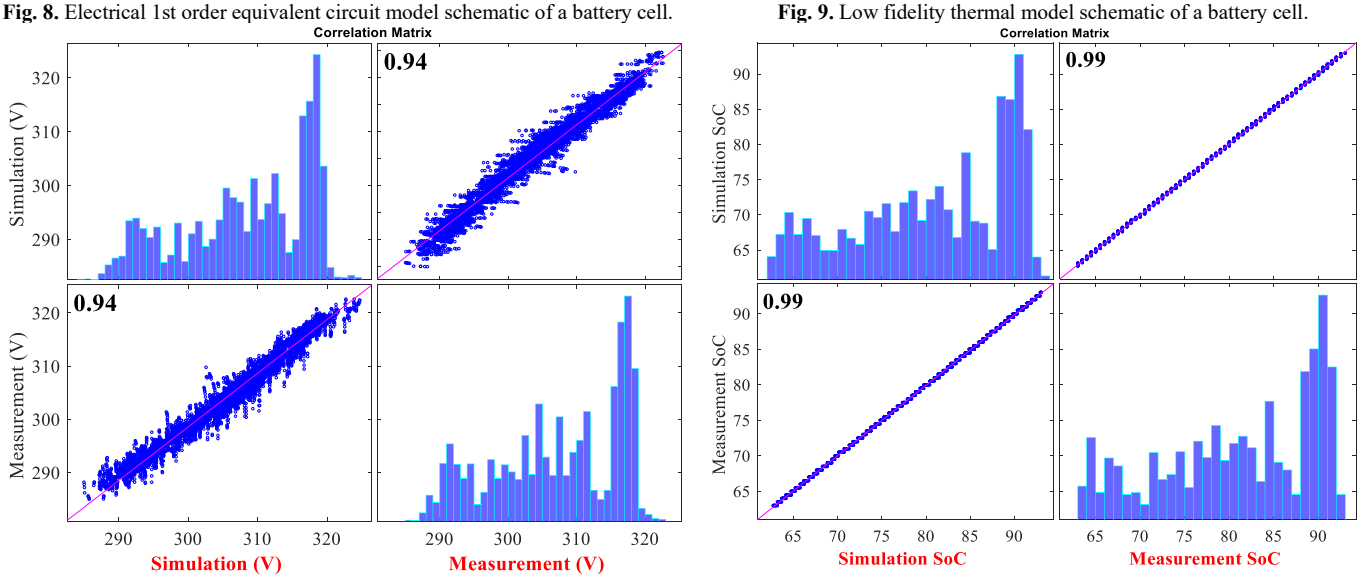
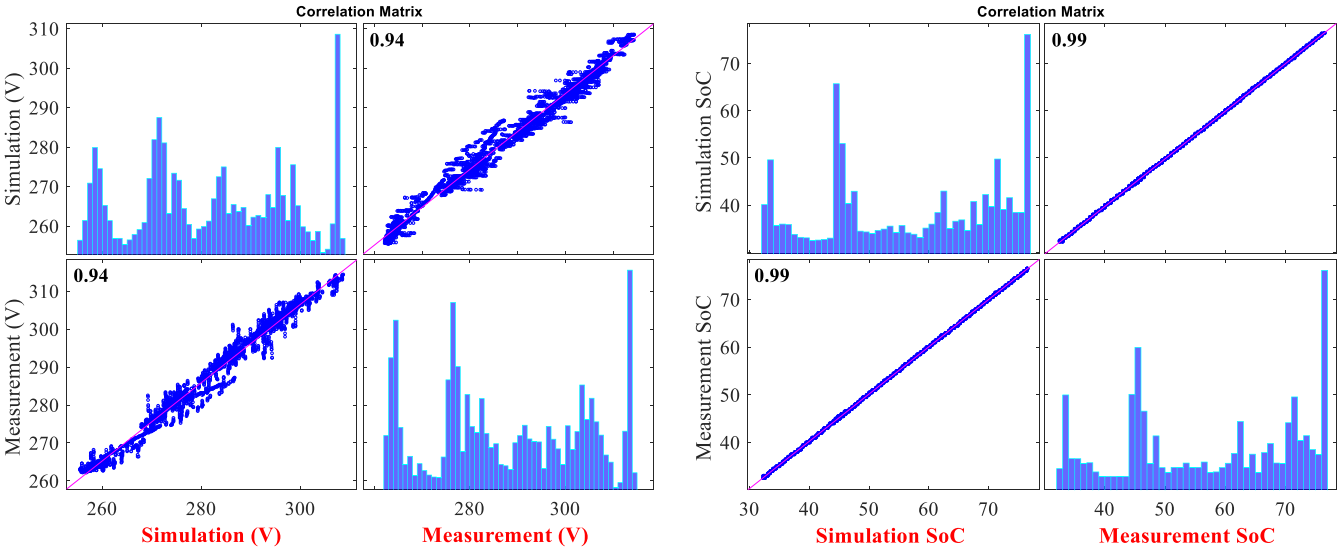


Fig. 9. Low fidelity thermal model schematic of a battery cell.



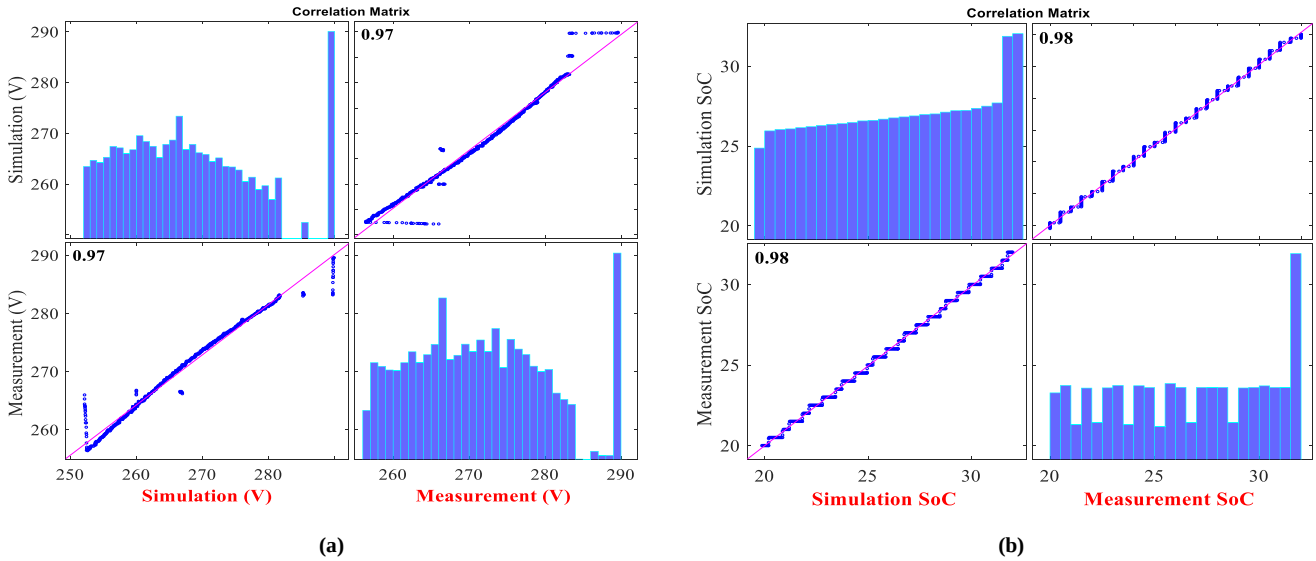
(a) (b)

Fig. 10. Extra-urban mission profile: Kendall's rank correlation between (a) Simulation battery pack voltage and RT-Measurement of battery pack voltage and (b) Simulation battery pack SoC and RT-Measurement of battery pack SoC.



(a) (b)

Fig. 11. Urban mission profile: Kendall's rank correlation between (a) Simulation battery pack voltage and RT-Measurement of battery pack voltage and (b) Simulation battery pack SoC and RT-Measurement of battery pack SoC.



(a) **(b)**

Fig. 12. Continuous hill-climbing mission profile: Kendall's rank correlation between (a) Simulation battery pack voltage and RT-Measurement of battery Pack voltage and (b) Simulation battery pack SoC and RT-Measurement of battery pack SoC.

It can be seen from Fig. 10-Fig. 12. that a high level of correlation is obtained between the low fidelity battery pack model and the RT-measurement data for all three mission profiles (***minimal 94%, maximum 99%***), which validates the accuracy of the low-fidelity battery pack modelling approach.

In the context of this work, the battery pack provides an accurate device level loading factor to the HV DC/DC converter in correspondence to the three mission profiles. The battery itself accepts a load current [A] as input (typically computed by the VCU) and provides a terminal voltage [V], the DC/DC device level loading, as an output, amongst others (i.e., load power and coolant temperature).

D. EV Powertrain thermal system modelling

A radiator-fan-based system is used to control the powertrain thermal system (PWTS), which comprises the PECs (i.e., HV DC/DC, inverter) and electrical machine in a series loop. A fixed-displacement pump drives water through the cooling circuit, which applied the mass coolant flow rate *($m_{coolant}$)* in the PWTS. The heat generated from the powertrain components *(i.e., ΣP_{HVDC}, $\Sigma P_{inverter}$, $\Sigma P_{E\text{-}motor}$)* is absorbed by the coolant and dissipated through the radiator. Moreover, the ambient temperature *(T_{amb})* and the speed of the vehicle *(v)* influence heat exchanger behaviour where it regulates the speed of the airflow going into the radiator. The thermal characteristics of the PWT are heavily dependent on the rotational speed setpoints of the pump *(η_{pump})* and fan *(η_{Fan})*, which are adjusted by a simple PI control depending on the total heat generation rate of the powertrain ($\Sigma P_{HVDC} + \Sigma P_{inverter} + \Sigma P_{E\text{-}motor}$). Based on the thermal management system, the electrical drive is mainly applied to boosting and energy recuperation. The inlet coolant temperature *($T_{coolant}$)* for the IBC can be obtained from equations (1)-(2).

$$s_{IBC}.M_{HVDC}.\frac{dT_{coolant}}{dt} = -\sigma.A_{IBC}.(T_{coolant} - T_{r,in}) - \sum P_{cooling} + \sum P_{Total,HVDC} + T_{DC\_int} \quad (1)$$

$$s_{HE}.M_{HE}.\frac{dT_r}{dt} = -\sigma_{HE}.A_{HE}.(T_{r,in} - T_{amb}) - s_{HE}.T_{amb}.m_A \quad (2)$$

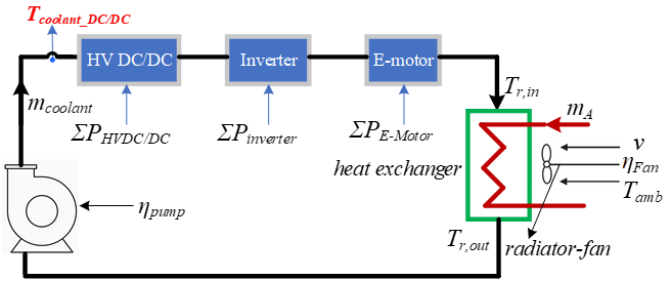


Fig. 13. Overview of the powertrain thermal system with two actuators.

Here the coefficients represent the HV DC/DC and heat exchanger's properties. Where s_{IBC}, s_{HE} are the specific heat capacities, M_{IBC}, M_{HE} denote the masses, T_M, T_A are the temperatures variation due to the masses, σ, σ_{HE} indicate the heat transfer coefficients, A_{IBC}, A_{HE} denote the cross-sectional area, $T_{r,in}$, $T_{r,out}$ represent the inlet, actual and outlet temperature of the radiator respectively, $P_{cooling}$ is the cooling power, T_{DC_int} is the initial temperature, m_A is the airflow, which is influenced by vehicle speed and the pump characteristics and $P_{Total,HVDC}$ is the total losses of the HV DC/DC converter. All the design parameters of the PWTS are taken from the OEM. The generic PWT platform for the BEV has been modelled as presented in Fig. 13; here, the inlet temperature sensor position is denoted in red ($T_{coolant}$).

In the context of this work, the inlet coolant temperature profiles due to separate mission profiles are used as device-level loading factors for the lifetime estimation of the HV DC/DC converter.

E. Interleaved DC/DC converter structure and control

As per a detailed review of the HV DC/DC converter [41], a 2-level 3-phase Interleaved Bidirectional HV DC/DC Converter (IBC) is the best suitable candidate for the high-power BEV applications (*≥30 kW*), as depicted in Fig. 14. The phase difference between interleaved switches is 120^0 due to 3-phase operation, which is applied to reduce the converter power density and input current ripple.

TABLE 4. PARAMETERS OF THE IBC.

Converter Parameters	Values
Inductance [L]	175.5 µH
○ Inductor Core	AMCC-core material
○ Inductor resistance [R_L]	2.53 mΩ
Output Capacitance [C]	160 µF
○ ESR [R_C]	1.80 mΩ
Operational switching frequency [f_{sw}]	60 kHz
Semiconductor power module	1.2 kV, 13 mΩ, 150 A
Cooling Method	50%-50% water glycol

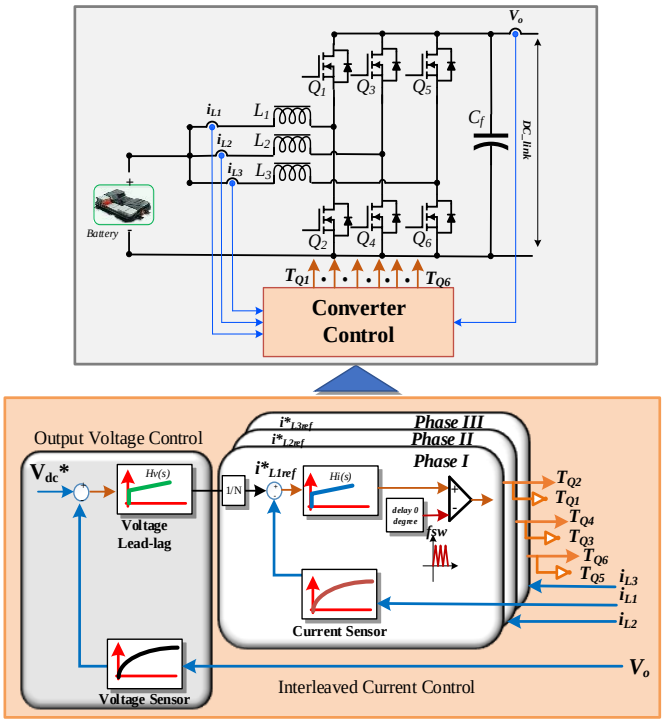


Fig. 14. The detailed IBC schematic diagram with dual-loop lead-lag controller structure. *Hv(s)* and *Hi(s)* represent the voltage and current controller's transfer functions. Here, L_1=L_2=L_3=L=175.5 µH and C_f=160 µF.

The interleaving technique allows the IBC to operate even at reduced power due to the battery cell failure. Hence, in EVs, the IBC modularity helps the EM to function even under cell-defective conditions, prolonging the BEV life and improving overall safety. Furthermore, the interleaving technique provides switch redundancy in the converter system. In this study, one complete phase failure redundancy condition is evaluated. The design parameters of the IBC are depicted in Table 4, and are formulated using a multi-objective genetic algorithm optimization tool mentioned in [42].

In this paper, a dual-loop type-II k factor-based control is used; it has a faster internal current-controlled loop that follows the reference current generated via a slower outer voltage loop, and the slower voltage loop is used to track the DC-link voltage as shown in Fig. 14. The cut-off frequency (f_c) of the voltage controller loop ($H_V(s)$) is 400Hz, while f_c is 4.5kHz in the current controller loop ($H_i(s)$).

A generalized small-signal averaged switch model of the IBC is used to design the control law for both boost and buck mode operation, as mentioned in [43]–[45]. The compensated type-II current-loop controller ($C_{i\text{-}boost}(s)$, $C_{i\text{-}buck}(s)$) and voltage-loop controller ($C_{v\text{-}boost}(s)$, $C_{v\text{-}buck}(s)$) transfer functions are depicted in Table 5 and equations (3)-(5).

TABLE 5. TYPE-II K-FACTOR BASED CONTROLLER'S TRANSFER FUNCTIONS (S).

Controller Type	Mode selection	Compensated controller's TF(s)	Eq. no
Current loop	Boost	$C_{i-boost}(s) = \frac{s+4634}{3.2e^{-3}s^2+167.2s}$	(3)
	Buck	$C_{i-buck}(s) = \frac{s+5351}{2.1e^{-3}s^2+133.5s}$	(4)
Voltage loop	Boost	$C_{v-boost}(s) = \frac{s+2504}{2.5e^{-4}s^2+0.972s}$	(5)
	Buck	$C_{v-buck}(s) = \frac{s+5351}{2.1e^{-4}s^2+0.3891s}$	(6)

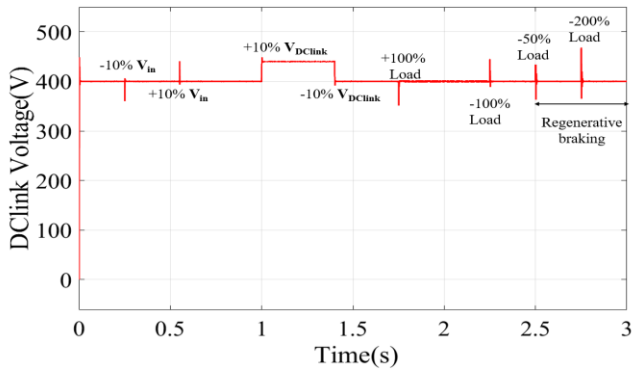


Fig. 15. Controller's response of the IBC to the disturbance in the input voltage at 0.25 sec and 0.55 sec (±10% step), output reference voltage at 1 to 1.4 sec (±10% step) and load changes at 2 s (60 kW), 2.2 s (30 kW), 2.4 s (-15 kW) and 2.7 s (-45 kW).

The robustness of the controller response has been verified for various disturbances, such as: battery voltage (*±10%* step), DC-link voltage (*+10%* step), and load fluctuations from *100%* to *200%* to *-100%* to *-50%* to *-200%* (*30 kW→60 kW →30 kW→-15 kW→-45 kW*). The DC-link voltage response of the IBC to the given fluctuations is illustrated in Fig. 15.

F. Detailed Electro-thermal modelling and validation of the IBC at full load condition

Detailed electrothermal modelling techniques for power semiconductor devices can be categorized into five types based on literature: *(a)* behavioural model [26], [46], [47], *(b)* physical model [48], [49], *(c)* semi-physical model (i.e., PSpice or SaberRD/ SaberEXP) [50]–[52], *(d)* numerical model (i.e., numerical tools such as ISE TCAD and MEDICI) [53], [54] and *(e)* semi-numerical model [55]. The physical models are represented by the composition of the internal layers of the semiconductors [48], [49]. They are accurate, but precise information about the internal structure of the device is required during modelling. Manufacturers usually do not give this information. Furthermore, they are time-consuming to simulate, so these models have not been preferred for mission profile-oriented simulations. Semi-physical models are used to analyse the conduction and switching behavior of the semiconductors [50]–[52]. The models are accurate but highly nonlinear due to the voltage dependency of equivalent capacitances presented in the semiconductor structure. Hence, the simulation speed is slow because the switching behavior needs to be simulated in detail. The numerical models in [53], [54] also have a high computation time due to the required settings of material performance and the geometry size of the devices. Furthermore, the semi-numerical models in [55] are based on geometrical microstructure parameters and composite elastic properties that are obtained using finite element analysis (FEA); hence, this type of model is not a potential candidate for

mission-profile-oriented simulations. Therefore, in this paper, the behavioural model of a SiC power module is used by extracting the characteristic curves of the equivalent MOSFET/diode from the manufacturer's datasheet. It is also known as a datasheet-driven modelling approach that introduces more nonlinear characteristics curves and more operating conditions to improve the accuracy of the DUT. The behavioural model can be implemented by either mathematical fitting or look-up tables (LuT), without considering the complicated physical operation mechanisms of the device. Furthermore, this type of model is accurate enough to allow modelling the electrical and thermal behavior of the semiconductors in detail without compromising the simulation speed [24].

The behavioural model of the SiC power module has been utilised in this paper for modelling the electro-thermal behaviour of the semiconductors, as following [26], [46], [47]. The idea consists basically of implementing the semiconductors as ideal switches and estimating in parallel their power losses. The total losses of MOSFET (P_{total_MOS}) comprise the switching losses (P_{sw_MOS}) and conduction losses (P_{cond_MOS}), and the total losses of the anti-parallel body diode of the power module (P_{total_Dio}) comprise the conduction losses (P_{cond_Dio}) and reverse recovery losses (P_{sw_RDio}). The total losses of the power module feed into the thermal module to estimate the MOSFET or diode junction temperature T_j and heatsink temperature T_H. Finally, the junction temperature T_j is then fed back to the loss's models of MOSFET or Diode to generate the impact of the temperature on the losses model. Instantaneous conduction and switching losses modelling are described in the following paragraphs.

The MOSFET is modelled as a gate *(G)* controlled ideal switch with an on-resistance *($R_{DS,on}$)* connected in series. The conduction voltage drop $V_{DS}(I, T_j)$ is modelled as a 2-D LuT, which is dependent on the mean flowing current ($i_{DS}(t)$) and junction temperature (T_j) of the SiC MOSFET. Hence, the instantaneous conduction losses of a MOSFET is expressed by equation (7).

$$p_{cond\_MOS}(I,T_j) = V_{DS}(I,T_j).i_{DS}(t) \tag{7}$$

The anti-parallel body diode of the MOSFET power module is modelled through the series connection of a voltage drop $V_{th}(I,T_j)$ and an on-resistor (R_{on}). Both of them can be modelled as 2-D LuT forward current ($i_F(t)$)-junction temperature (Tj) dependent elements. The instantaneous conduction losses of a body diode can be calculated by (8).

$$p_{cond\_D}(I,T_j) = V_{th}(I,T_j).i_F(t) \tag{8}$$

The switching losses appear during the turn-on and turn-off transition of the semiconductors due to their non-ideal voltage and current transitions, which produce an eventual coexistence of voltage and current. In order to avoid high computational cost simulations, this paper considers turn-on and turn-off commutations of the MOSFET as ideal transitions while ignoring the transient overvoltage response. In this paper, a 3D-LuT is considered, which couples actual drain-source voltage v_{DS}, conducted current i_{DS} and junction temperature *Tj*. However, the energy losses are estimated based on linear approximations between the actual and reference drain-source voltage and current response. The reference drain-source voltage and current are represented as $V_{DS,ref}$ and $I_{DS,ref}$, switching loss dependency coefficients for voltage and current are l_v and l_i. The instantaneous average switching losses of a MOSFET can be obtained by equation (9).

$$p_{sw,MOS} = f_{sw}.\left[E_{MOS\_on}\left(\left(\frac{v_{DS}}{V_{DS,ref}}\right)^{l_v},\left(\frac{i_{DS}}{I_{DS,ref}}\right)^{l_i},T_j\right) + E_{MOS\_off}\left(\left(\frac{v_{DS}}{V_{DS,ref}}\right)^{l_v},\left(\frac{i_{DS}}{I_{DS,ref}}\right)^{l_i},T_j\right)\right] \tag{9}$$

The switching losses in the body diode occur mainly at diode turn-off due to the reverse recovery of the charge stored in the junction capacitance. The switching losses in the Diode are shown in equation (10), considering the energy turn-off E_{D_off}, a 3D-LuT coupled with actual blocking voltage v_F, conducted the current i_F, and junction temperature *Tj*. Here, again a linear approximation is used between the actual and reference blocking voltage $V_{F,ref}$ and current response $I_{F,ref}$.

$$p_{sw\_D} = f_{sw}.\left[E_{D\_off}\left(\left(\frac{v_F}{V_{F,ref}}\right)^{l_v},\left(\frac{i_F}{I_{F,ref}}\right)^{l_i},T_j\right)\right] \tag{10}$$

The LuT data can be obtained from the specific double pulse test (DPT) measurement or manufacturer datasheet. In this paper, corresponding characteristic curves are taken from the particular device datasheet.

The total losses in the IBC comprise of MOSFET losses (switching losses, conduction losses and reverse recovery losses), inductor losses (core loss, air-gap loss and conduction loss) and ESR losses of the DC-link capacitor. The calculation of inductor and capacitor losses is derived in equations (11)-(15). The core geometry of the inductor is taken from the datasheet [56]. The internal resistance of inductor Litz wire (rectangular HF 299) and ESR are used to calculate the passive components conduction losses [56], [57].

$$P_{loss\_inductor} = P_{Core} + P_{air-gap} + P_{CondL} \tag{11}$$

with

$$P_{condL} = I_{RMS,L}^2 R_L \tag{12}$$

$$P_{core} = W_{core}\left(K_a K_b f_{sw}^{\alpha y} \Delta B_{max}^{\beta x}\right) \tag{13}$$

$$P_{air-gap} = k_{gap}.d.l_g.f_{sw}.\Delta B_{max}^{\beta x} \tag{14}$$

$$P_{Cap} = \sum_{i=1}^{n} ESR(f).I_{RMS,C}^2(f) \tag{15}$$

Where $I_{RMS,L}$ represents the instantaneous rms current of the inductor, R_L is the resistance of the Litz wire, W_{core} is the inductor core weight, K_a, K_b, αy and βx are the C-shaped core loss coefficients, f_{sw} is the switching frequency, the maximum AC-flux density at the rated condition is ΔB_{max}, gap loss coefficient is k_{gap}, inductor's core depth factor is *d*, airgap coefficient of the core is l_g, $I_{RMS,C}$ is the instantaneous rms current of the DC-link capacitor and *ESR* is the equivalent series resistance of the DC-link capacitor.

The main assumption is the unidirectional heat-flow from the device junction to the case, through the thermal interface material (TIM) grease, then to the heatsink, and finally heatsink to the coolant. In this paper, the detailed thermal impedance network of the half-bridge power semiconductor module for each leg, thermal impedance network of the TIM, thermal impedance network of the liquid-cooled heatsink and mission profile-based coolant behaviour have been considered as illustrated in Fig. 16.

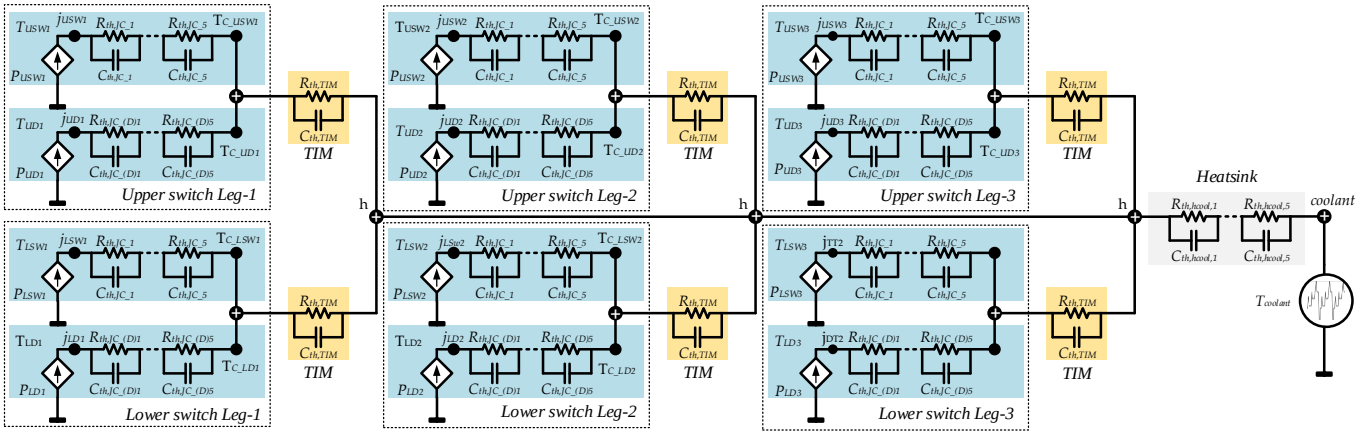


Fig. 16. Detailed thermal impedance network of the IBC; here the semiconductor's thermal circuit is marked with a blue colour area, TIM's thermal circuit area is marked with yellow colour and heatsink thermal circuit area is marked with ash colour.

The dynamic thermal modelling for the power semiconductors is designed using Foster lumped network ($R_{th(JC)}$-$C_{th(JC)}$), which is composed of a junction-to-case thermal resistance $R_{th(JC)}$ and junction-to-case thermal capacitance $C_{th(JC)}$. Multi $R_{th(JC)}$-$C_{th(JC)}$ lumps represent different layers of materials from the chip to the case of the semiconductor device. The junction of MOSFET (or Diode) is represented by thermal sources governed by the MOSFET (or diode) instantaneous power losses. In this paper, a fifth-order Foster thermal network is implemented using thermal parameters extracted from the manufacturer datasheet. The time-domain thermal impedance of MOSFET (or Diode) is calculated as equation (16).

$$Z_{th(JC)n} = \sum_{i=1}^{5} R_{th(JC)\_M(D)i} \cdot \left(1 - e^{\frac{-t}{\tau_{Jci}}}\right) \tag{16}$$

It is noted that τ_{JCi} is the time constant and is a function of $R_{th(JC)\_M} \times C_{th(JC)\_M}$. The junction temperature $T_{J\_M(D)}$ of MOSFET (or Diode) can be estimated as (17)-(19).

$$T_{j\_M(D)} = T_{cs} + \Delta T_{JC\_M(D)} \tag{17}$$

$$\Delta T_{JC} = P_{n\_M(D)} \cdot Z_{th(JC)n} \tag{18}$$

$$T_{cs} = T_{hCool} + \Delta T_{ch}; \Delta T_{ch} = Z_{th(TIM)} \sum P_{n(M)} + P_{n(D)} \tag{19}$$

Where T_{cs} is the case temperature, $\Delta T_{JC\_M(D)}$ is the fluctuation of junction to case temperature, $P_{n\_M(D)}$ is the loss of individual component (MOSFET/diode), T_{hcool} is the heatsink temperature and ΔT_{ch} is the fluctuation of the case to heatsink temperature. Besides, $Z_{th,(TIM)}$ is the thermal network due to TIM between power module and heatsink and is a function of $R_{th,TIM} \times C_{th,TIM}$.

As thermal stress is one of the critical stressors of DC-link capacitor wire-out, the hot-spot temperature (T_{cap}) of the DC-link capacitor is estimated as using equation (20).

$$T_{cap} = T_{hcool} + P_{Cap} \cdot R_{ha} \left(1 - e^{\frac{-\Delta t}{\tau_{ha}}}\right) \tag{20}$$

Where R_{ha} is the thermal resistance of the capacitor, Δt is the temperature change of the capacitor, and τ_{ha} is the thermal time constant of the capacitor.

The heatsink dynamic thermal behaviour is determined by feeding constant power losses in the cooling network and measuring the temperature build-up at the coolant outlet. The ratio of the temperature difference between the coolant outlet and inlet concerning the power losses gives the thermal impedance. The order and magnitudes of Foster network parameters can be extracted using curve-fitting on the obtained data. A fifth-order Foster thermal network is implemented for the heatsink thermal assumption using vendor heatsink data as presented in equation (21) [58].

$$Z_{th,hCool} = \frac{R_{th,hcool,1}}{\tau_{th,hcool,1}s + 1} + \ldots\ldots + \frac{R_{th,hcool,5}}{\tau_{th,hcool,5}s + 1} \tag{21}$$

The heatsink temperature is estimated using the following equation (22).

$$T_{hCool} = T_{coolant} + Z_{th,hCool} \sum P_{Total} \tag{22}$$

Where $T_{Coolant}$ is the inlet coolant temperature from the PWT unit and P_{Total} is the total loss of the IBC.

In this paper, a liquid-cooled SiC-based *30 kW* IBC prototype has been used to verify the electro-thermal model of semiconductor devices, as shown in Fig. 17.

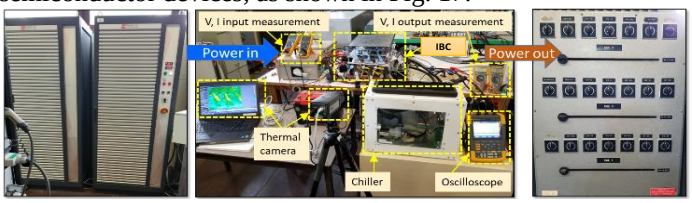


Fig. 17. A liquid cooled SiC-based experimental setup of the IBC for lifetime testing.

The efficiency is measured for power ratings from 0 to 25 kW for boost mode operation, while 0 to -28 kW for buck mode operation, using a highly accurate *Yokogawa WT3000* power analyser *(~0.02% accuracy)*.

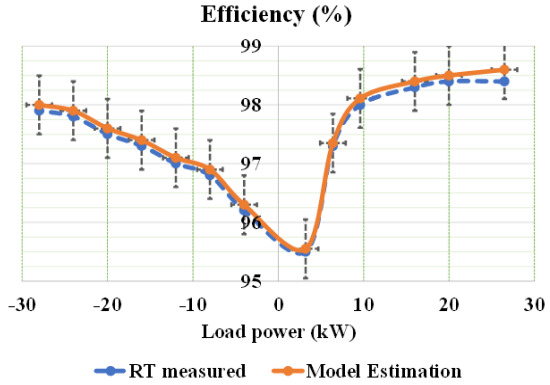


Fig. 18. Efficiency comparison between real-time measurement and estimated model, while RT measurement are taken using a YOKOGAWA WT1804E power analyser and error bar is showing 0.50% of the error limit.

According to the obtained results presented in Fig. 18, an excellent accuracy is found between the experimental measurement and the model estimation. The largest Mean Percentage Error (*MPE*, the MPE equation is depicted in the Appendix) observed is approximately *0.2%* between the measured efficiency and model estimation during full-load operation.

III. Mission Profile Oriented Component-Level Lifetime Estimation

For lifetime estimation of the IBC, a holistic stepwise process must be followed, as presented in Fig. 19. Basically, the above-mentioned mission profiles need to be translated into the thermal stress function. Afterward, the thermal stress is converted into the damage accumulation estimation.

A. Mission-profile to thermal stress translation

In this paper, the load profile comprises the NMC battery pack voltage, the dynamic load power of the inverter, and the inlet coolant temperature of the IBC converter. Then, taking into account that the instantaneous controlled current conducts through the MOSFET power module, both conduction (power) and switching (energy) losses are analytically estimated in parallel calculations. From these calculations, the average power losses in the MOSFET power module during a switching period can be easily approximated by means of quasi-ideal elements. Later, the power losses of the components are utilized as input to thermal models to acquire the thermal stress during the mission profile operation.

B. Thermal stress to cycle counting translation

The junction temperature of the MOSFET power module and hot-spot temperature of the capacitor are varied according to the mission profile variation. Thermal stress leads to fatigue failure of the power electronics components in the PECs. Hence, after obtaining the thermal stress profile, a rainflow counting algorithm is used to count the number of cycles (n_i), the amplitude of the temperature swing (ΔTj), the pulse duration of MOSFETs (t_{ON}) and mean junction temperature (T_{jm}). The rainflow cycle counting statistically translates the instantaneous thermal stress profile into the regular thermal cycle.

C. Component-level lifetime estimation

The outputs of the rainflow cycle counting algorithm, namely ni, ΔTj, T_{jm} and t_{ON} are then inputted into the LESIT *(Leistungs Elektronik Systemtechnik und Informations Technologie)* parameter-based lifetime estimation model to determine individual component lifetime. In this paper, the LESIT parameters are considered based on the SKiM 63 lifetime model from Semikron [58]. Furthermore, under specific electro-thermal stress conditions, the number of cycles to failure (N_f) is also influenced by the bond wire aspect ratio (a_r) and the body diode impact factor (f_{diode}). For the lifetime estimation of the SiC power module, the established lifetime model known as Scheuermann's model [59] is used in this paper.

$$N_f = A \times (\Delta T_j)^{\alpha} \times (ar)^{\beta_1 \cdot \Delta T_j + \beta_0} \times \left[\frac{C + (t_{ON})^{\gamma}}{C+1}\right] \times e^{\left(\frac{E_a}{k_b \times T_{jm}}\right)} \times f_{diode} \quad (23)$$

Where A is the technology factor, α, β_0, β_1, γ and C are the model parameters, as depicted in Table 6, E_a is the activation energy and k_b is the Boltzmann constant.

As SiC power devices are only recently seeing widespread commercial use, comprehensive data on power cycling testing of SiC power devices are not readily available from PE manufacturers. Hence, even though the parameters for SiC-based semiconductors, shown in Table 6, can be acquired from the SKiM 63 lifetime model [58], complete degradation and lifetime models are still to be developed for the SiC power modules. Therefore, the LESIT model of Si-based IGBT modules is applied for the SiC devices to demonstrate the proposed stepwise methodology. The lifetime estimation results obtained using the proposed method can be interpreted as relative assessment and for comparison only; however, procedures exemplified in the proposed assessment method are still valid.

In this paper, for lifetime estimation of the polypropylene DC link capacitor, the Arrhenius model in [60] is used, as presented in equation (24), which is basically a medium stress factor-based model on voltage and temperature fluctuations.

$$L_c = L_f \times e^{\left[\left(\frac{E_a}{k_b}\right)\left(\frac{1}{T} - \frac{1}{T_f}\right)\right]} \times \left(\frac{V}{V_f}\right)^{-n} \quad (24)$$

Where L_f and L_c are the time-to-failure at the testing condition and actual condition, V_f and V are the DC-link voltage at the rated condition and actual condition, T_f and T are the temperatures at the testing condition and rated condition and n represents the medium voltage stress factor. In this paper, a *type 947C* polypropylene DC-link capacitor (*160µF)* has been considered for lifetime estimation.

Typically, the lifetime of a power device is calculated in terms of total lifetime consumption, which is basically the accumulation of damage over the device's lifetime and is dependent on the mission profile that the device is subjected to. In this paper, the Miner's linear damage accumulation rule is applied for LC_{sw} calculation [59], as shown in equation (25).

$$LC_{sw} = \sum_{i=1}^{k} \frac{n_i}{(N_f)_i} \quad (25)$$

Where n_i is the number of cycles during specific thermal stress (i.e., T_{jm}, ΔT_j and t_{ON}), while $(N_f)_i$ expresses the number of cycles to failure at that operating point.

Equation (26) describes a similar accumulated ageing calculation of the DC-link capacitor (LC_{cap}).

$$LC_{cap} = \sum_{t=1}^{t} \frac{\Delta L_c}{L_{c,t}} \quad (26)$$

Table 6. Parameters of the Lifetime Model [58].

Parameters	Unit	Value	Testing conditions
A	[-]	*3.4368×10^14*	-
α	[-]	*-4.983*	$64^0C \leq \Delta T_j \leq 113^0C$
β_1	[-]	*-9.012×10^-3*	$0.19 \leq ar \leq 0.42$
β_0	[-]	*-1.942*	$0.19 \leq ar \leq 0.42$
C	[-]	*1.434*	$0.07s \leq t_{ON} \leq 63s$
γ	[-]	*-1.208*	-
f_{diode}	[-]	*0.6204*	-
a_r	[-]	*0.31*	-
E_a	[eV]	*0.06606*	$32.5°C \leq T_{jm} \leq 122°C$
k_b	[eV/K]	*8.61733×10^-5*	-
L_f	[h]	*5,000*	*@ 85^0C*
T_f	[K]	*358*	-
V_f	[V]	*1200*	*DC*

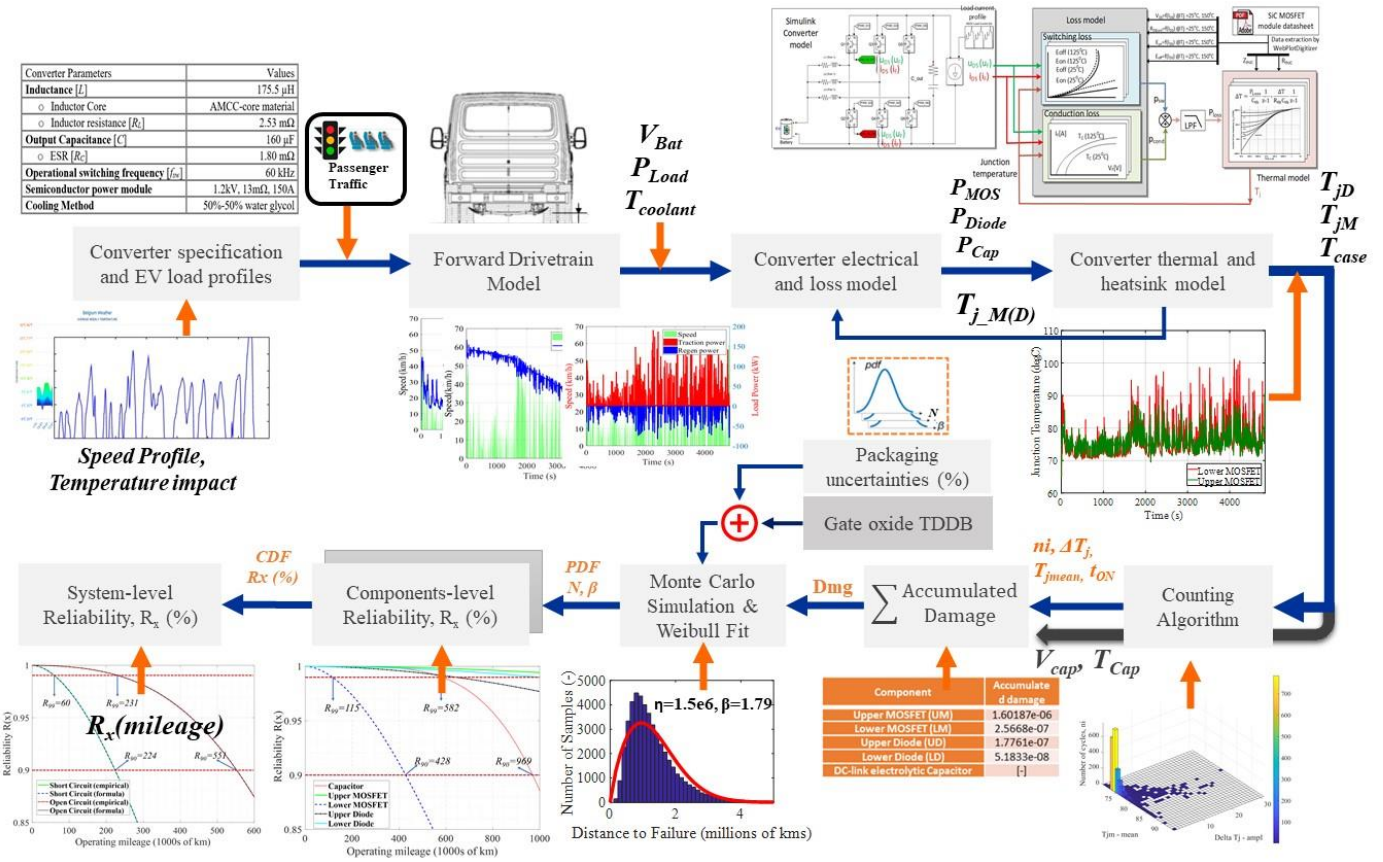


Fig. 19. Stepwise real-life mission profile-oriented lifetime estimation method of the IBC for the EV drivetrain applications.

Where ΔL_c is the instantaneous lifetime at specific thermal stress and $L_{c,t}$ corresponds to the total lifetime at that particular condition. The lifetime equations in (25)-(26) express the device-level loading impact on the damage and the linearly accumulated total damage. When either LC_{sw} or LC_{cap} exceeds 1, the IBC is considered to reach the end of its operating life.

IV. Lifetime Estimation (Case Study)

In this section, the lifetime estimation investigated in section III is applied to the IBC as shown in Fig. 14, and the parameters of the IBC are depicted in Table 4. A *1.2 kV, 13 mΩ* all-SiC half-bridge power module from a prominent vendor is utilised. The SiC module comprises six parallel second-generation SiC MOSFET dies, and 12 anti-parallel SiC Schottky diode dies. The SiC half-bridge consists of an upper MOSFET switch, a lower MOSFET switch, an anti-parallel SiC Schottky lower Diode and an upper Diode [61].

A custom-made liquid-cooled 50%-50% water-glycol (anti-freeze) heatsink is designed to retain maximum junction temperature under 145^0C at severe operating conditions (*80 kW*) to ensure the safety margin of the IBC operation. Furthermore, a type *947C* polypropylene DC link capacitor from a leading manufacturer is considered to ensure low-temperature rise thanks to offering low DC-link ripple and ESR.

Mission profiles of three distinct characteristics from an automotive OEM are taken into consideration to investigate the impact of different missions on an automotive IBC's lifetime. Using the proper parameters of the OEM drivetrain, the loading factors for the IBC are formulated, as depicted in Fig. 4-Fig. 6. The thermal stressors of the half-bridge power module and DC-link capacitor are evaluated for their corresponding accumulated damage.

A. Thermal loading of the IBC at different mission profiles

The IBC half-bridge power module thermal stress loading at the **extra-urban cycle** is presented in Fig. 20. The thermal stressors of the IBC are given as inputs to the cycle counting algorithm. Using the rainflow algorithm, the range of temperature swing (ΔTj), mean temperature T_{jm}, and corresponding depths and averages of the cycle are decomposed.

The highest number of cycles (1500 cycles) has occurred at a mean temperature of 72^0C in the lower MOSFET during the extra-urban mission profile operation. In contrast, the upper MOSFET, upper Diode, and lower Diode mean temperatures are approximately 72^0C. The exact number of cycles is dependent on the imposed stress on the MOSFET/Diode during the operation of the mission profile. It can be seen from Fig. 20 that the lower MOSFET experienced the highest number of cycles (1500 cycles) during the extra-urban mission profile operation, which reveals that the lower MOSFET is the most failure-prone component in the SiC power module. In addition, the upper MOSFET has experienced the lowest number of cycles during this mission profile operation, which indicates that the upper MOSFET will have the highest lifetime.

It can be seen from Fig. 21 that the lower MOSFET experienced the highest number of cycles (185 cycles) during the **urban mission profile** operation.

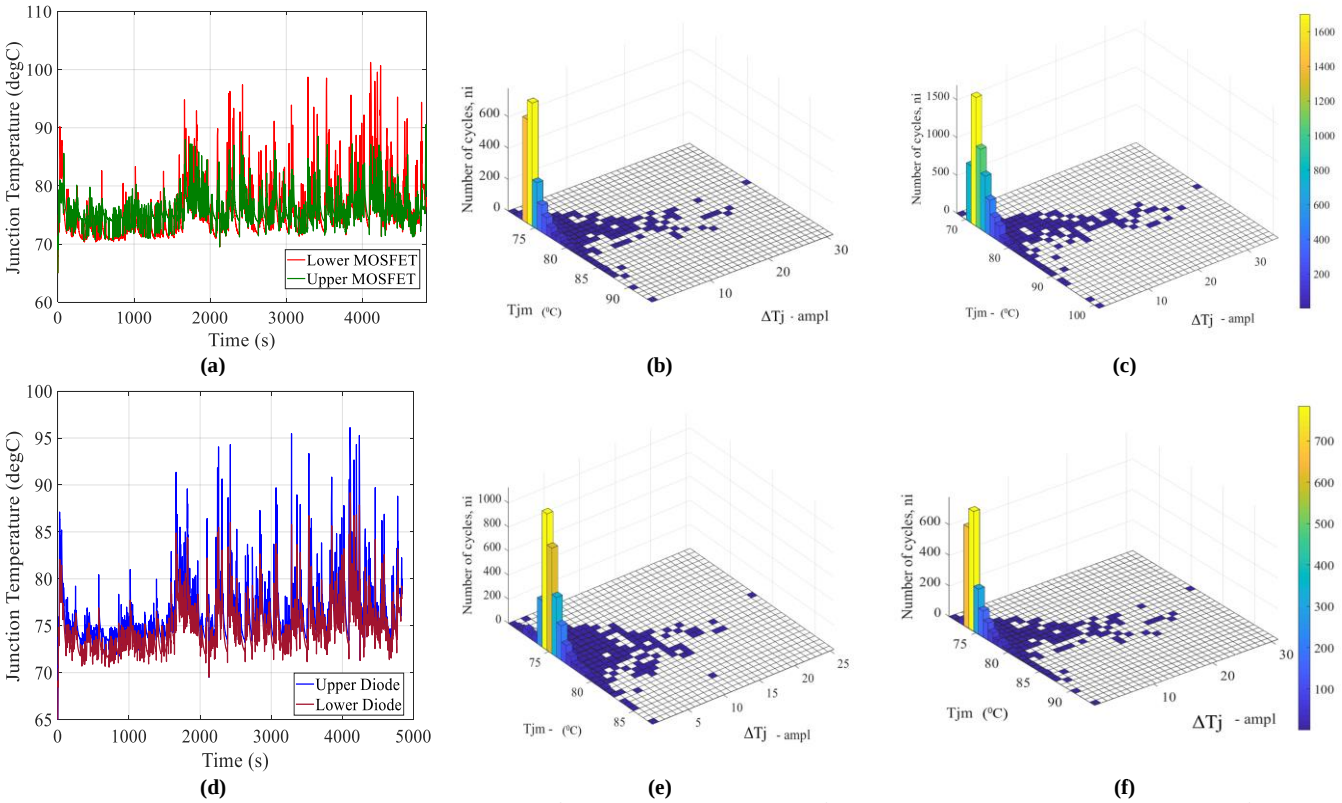


Fig. 20. Thermal stress loading during ***Extra Urban mission profile***: (a) junction temperature of both MOSFETs and (d) junction temperature of both Diodes; Rainflow cycle counting results → Number of Cycles (*ni*), Mean junction temperature Tjm (K) and Temperature swing Delta Tj (K) during ***Extra Urban mission profile***: (b) Upper MOSFET, (c) Lower MOSFET, (e) Upper Diode and (f) Lower Diode.

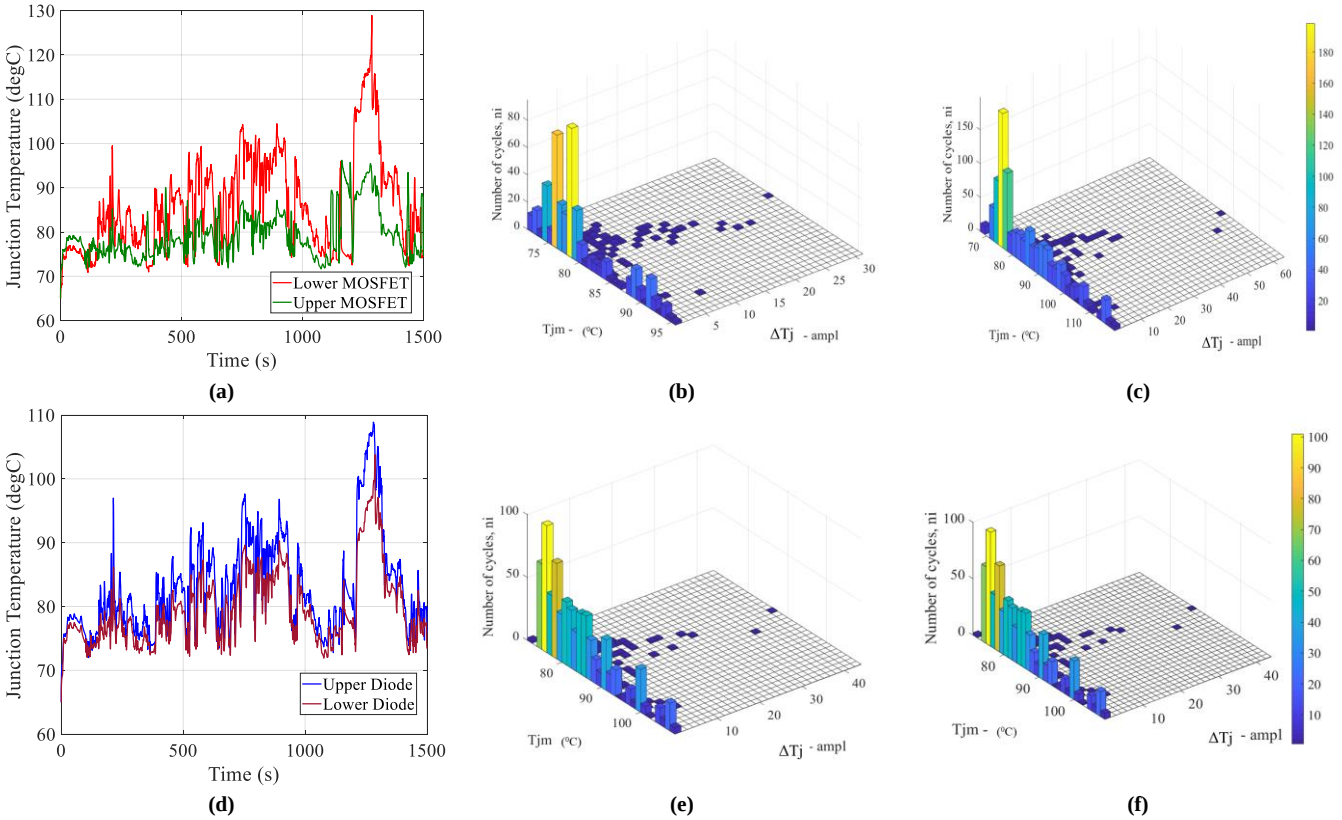


Fig. 21. Thermal stress loading during ***Urban mission profile***: (a) junction temperature of both MOSFETs and (d) junction temperature of both Diodes; Rainflow cycle counting results → Number of Cycles (ni), Mean junction temperature Tjm (K) and Temperature swing Delta Tj (K) during ***Urban mission profile***: (b) Upper MOSFET, (c) Lower MOSFET, (e) Upper Diode and (f) Lower Diode.

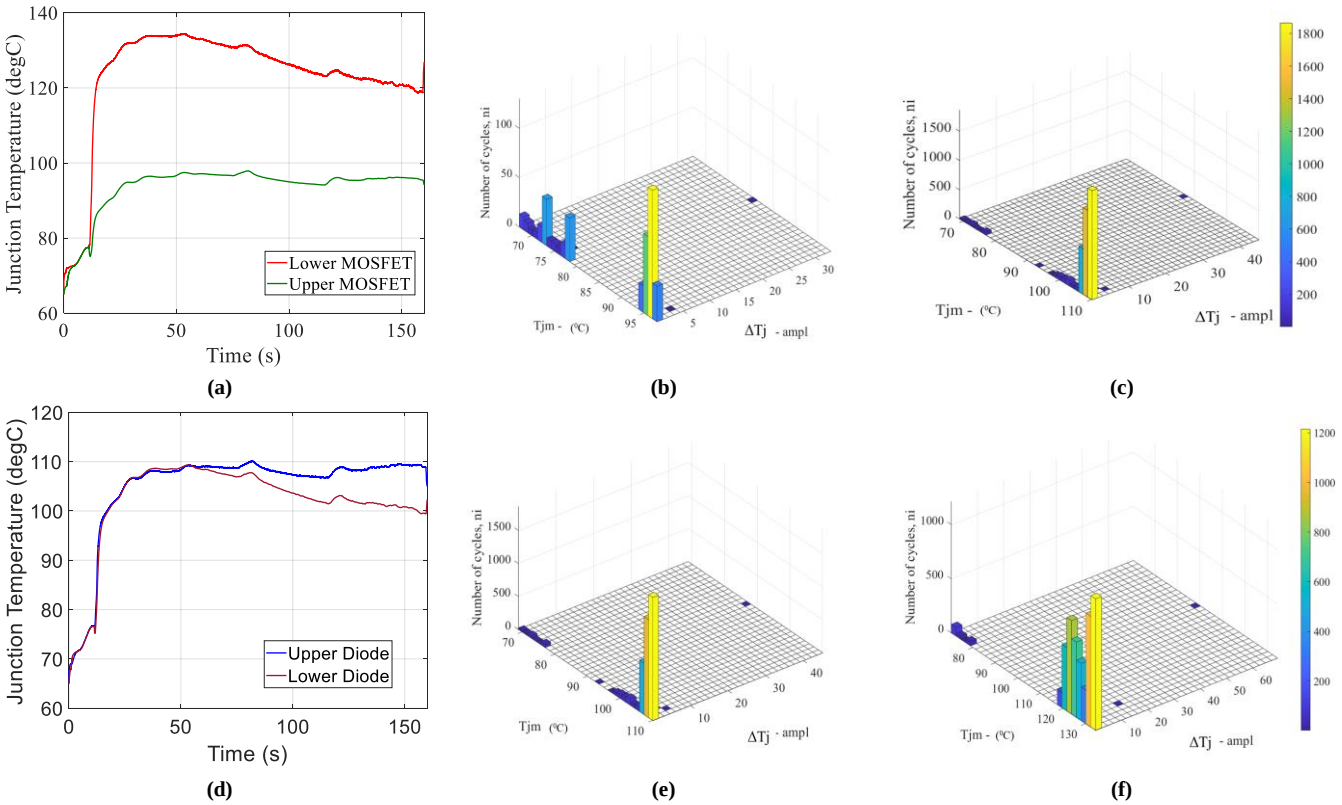


Fig. 22. Thermal stress loading during ***Continuous Hill climbing profile***: (a) junction temperature of both MOSFETs and (d) junction temperature of both Diodes; Rainflow cycle counting results → Number of Cycles (ni), Mean junction temperature Tjm (K) and Temperature swing Delta Tj (K) during ***Continuous Hill climbing profile***: (b) Upper MOSFET, (c) Lower MOSFET, (e) Upper Diode and (f) Lower Diode.

However, the total cycle number is lower than that of the extra-urban profile, which reveals that stress applied to the PE components during the urban mission is higher than stress applied during the extra-urban mission. Moreover, the lower MOSFET is the most failure-prone component, and the upper MOSFET has the highest lifetime throughout this mission.

Finally, it can be seen from Fig. 22 that the lower MOSFET experienced the highest number of cycles during the **hill-climbing mission profile** operation, which reveals that the lower MOSFET is the most failure-prone component in the SiC power module. However, the number of cycles is negligible compared to the previous two cycles as the operating cycle is very limited (160 sec), which means there is less chance of failure. Hence, it is concluded that the hill-climbing cycle does not contain sufficient data points to estimate the lifetime accurately.

V. System-Level Lifetime Estimation

To make a more complete analysis, the intrinsic effects of dielectric breakdown on the lifetime estimation of the IBC are also investigated, which is modelled as a series association with mission-profile based component-level LESIT modelling.

A. Intrinsic reliability of SiC MOSFET power module

Like any semiconductor devices, the SiC-based devices also suffer from a breakdown in the gate oxide over time; for accurate lifetime estimation, the intrinsic lifetime estimation factors need to be integrated, i.e., the TDDB linked to the oxide layer, and more particularly to the SiC power module [62]. The TDDB failure is independent of mission profile. Instead, it is dependent on the time that SiC MOSFET's gate oxide is exposed to a given voltage [63].

Hence, in this paper, the manufacturer reported the meantime to failure (MTTF) due to the dielectric breakdown of Gen2 SiC MOSFETs for different gate voltages have been utilized, as illustrated in Fig. 23 [64].

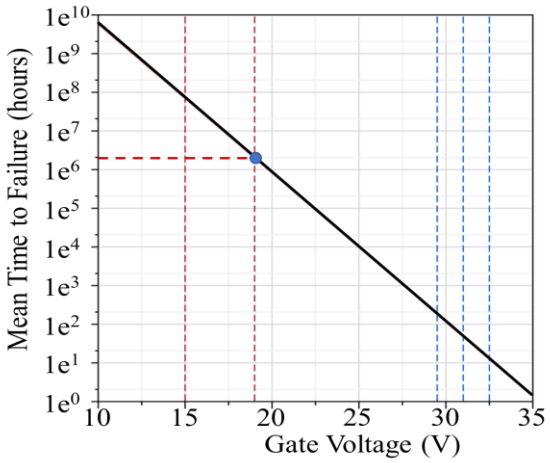


Fig. 23. Effect of the TDDB on the MTTF of SiC MOSFET power module [64].

The effect of TDDB on individual half-bridge power modules within the IBC is investigated in this paper for an 18.5 V gate voltage. Similar data also exist in the literature for device failures in the 10th and the 90th percentiles range. A Weibull approximation is prepared to simulate the effects on device-level lifetime due to the TDDB [64]. The impact of TDDB on the lifetime of the power module is independent of the other

stress factors that affect such semiconductor power electronic devices. Thus, the lifetime of the power module is a combination of the reliability due to the TDDB and the reliability determined according to the LESIT model in previous sections III and IV; the absolute lifetime estimation is modelled using series association.

B. *Lifetime estimation based on LESIT model parameters*

The previous sections III and IV dealt with finding the number of cycles and accumulated lifetime (*LC*) of the individual components for the specific set of operating conditions (i.e., real-life missions) by utilizing the rainflow algorithm. The lifetime determined in the previous sections assumed ideal conditions, where the parametric values used in the Arrhenius equation for the various components are precisely the same as mentioned in the manufacturer datasheet without considering any uncertainties. In reality, the manufacturer datasheet values are given as mean data points, and the actual value should vary from the mean with a certain standard deviation. This variation arises from packaging issues, i.e., minor faults, imperfections in the packaging process and variations in the stresses experienced. In this paper, to consider these packaging uncertainties during the lifetime assessment of the IBC system, a Monte Carlo analysis is utilized as packaging uncertainties are introduced in this statistical analysis as parametric variations [65]–[68]. Finally, to get the lifetime distribution of the IBC system concerning mileage, Monte Carlo values fit using the standard Weibull equation.

(a) Monte Carlo analysis

To perform a Monte Carlo analysis, random parameter variations should be introduced to the Arrhenius equation parameters [65]–[68]. The parameters describing the Arrhenius equation can be categorized into three types:

A. Mission profile-based parameters are those whose data points vary with time during the actual use of the IBC in a mission. In this paper, these values are found through the highly accurate IBC system simulation based on OEM mission-profiles scenarios. For Monte Carlo analysis, the mean and standard deviation of the output datasets are calculated, from which the dataset, with a normal distribution, is generated. Mission profile-based parameters include: ΔT_j, t_{ON}, T_{jm}, n_i, T, and V.

B. Non-mission profile-based parameters are those that are extracted from the datasheet of the components and are usually given by the OEM after dynamic tests and characterization. For non-mission profile-based parameters, the dataset for Monte Carlo analysis is generated in three ways. The first approach is: as the OEM supplies an upper and lower limit, between which the values of a given parameter can vary, then a random number dataset with a uniform distribution between those limits is generated for that parameter. The second approach is: the OEM gives the tolerance for that parameter, then a random number dataset with a normal distribution having as mean the parameter value, and a standard deviation that is a fifth of the specified tolerance are generated for the parameter. Finally, the third approach is: the OEM does not specify any tolerance or range limits for the parameter, then a random number dataset with normal distribution having the mean as the value of the parameter, and a standard deviation assumed to be 10% of the mean value is generated for that parameter. Non-mission-based parameters include A, α, ar, β_1, β_0, C, γ, E_a, f, n, V_f, T_f, and L_f.

C. Parameters that are physical constants and have been determined very precisely by the scientific community. These parameters are used as constants. Physical constants include k_b.

In this paper, Monte Carlo is performed for a population of 100,000 for three types of mission profiles, the Extra-Urban mission profile, the Urban mission profile and the Hill climbing mission profile. The non-mission profile-based parameter datasets are kept constant regardless of the mission, but the mission profile-based parameters-datasets have been varied according to the dynamic response of the mission profile. This enables a comparison of the lifetimes of the IBC when the vehicle is subject to different driving scenarios.

The resulting random dataset from the Monte Carlo analysis is then fit using Weibull distribution, whose probability density function is expressed as:

$$f(t,\beta,\eta) = \left(\frac{\beta}{\eta^{\beta}}\right).t^{(\beta-1)}.e^{-\left(\frac{t}{\eta}\right)^{\beta}} \quad for\ t \geq 0 \tag{27}$$

Where β is the shape parameter, η is the scale parameter, and t is the time duration. The shape parameter describes which phase of the "bathtub" curve the failure mode is a part of, as illustrated in Fig. 24. If $\beta < 1$, then the failure is mainly due to factory defects and decreases with time. $\beta = 1$ means that the product is within its useful lifetime, where failure occurs due to random chance at a constant rate. $\beta > 1$ means that the failure occurs due to the "wear out" of the product, which increases with time. The scale parameter corresponds to the time when 63.2% of the sample population will have failed; thus, it can be approximated as the median failure. The cumulative density function of the Weibull distribution, which defines the "unreliability," is given as:

$$CDF(t,\beta,\eta) = 1 - e^{-\left(\frac{t}{\eta}\right)^{\beta}} \quad for\ t \geq 0 \tag{28}$$

Thus, the reliability can be expressed as:

$$R(t,\beta,\eta) = e^{-\left(\frac{t}{\eta}\right)^{\beta}} \quad for\ t \geq 0 \tag{29}$$

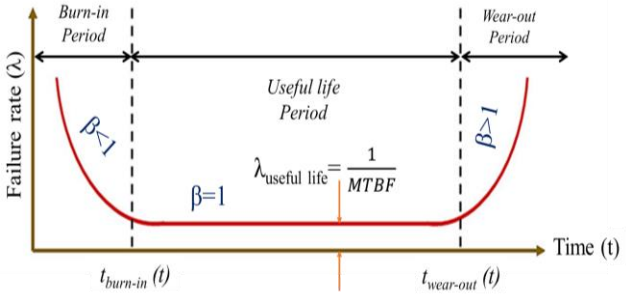
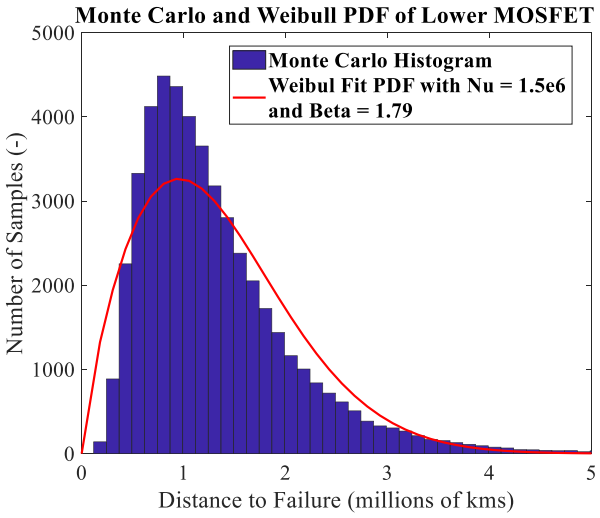


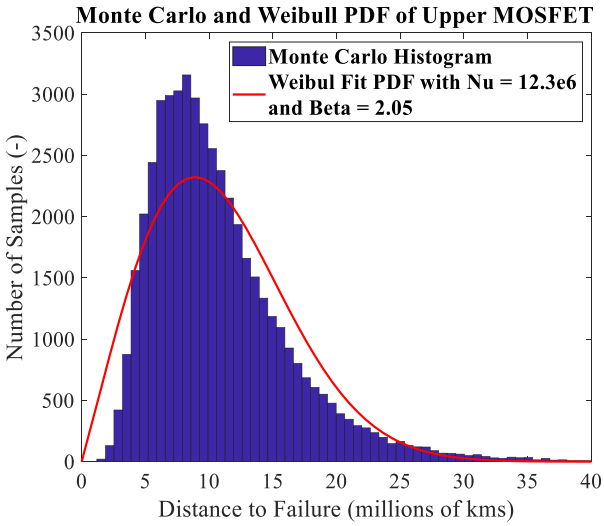
Fig. 24. The bathtub curve depicting the mode of failure at different periods.

Fig. 25 (a)-(e) illustrate the Weibull distribution from the Monte Carlo analysis (using *100,000* population samples) of the LESIT model of the components of the IBC under test, namely

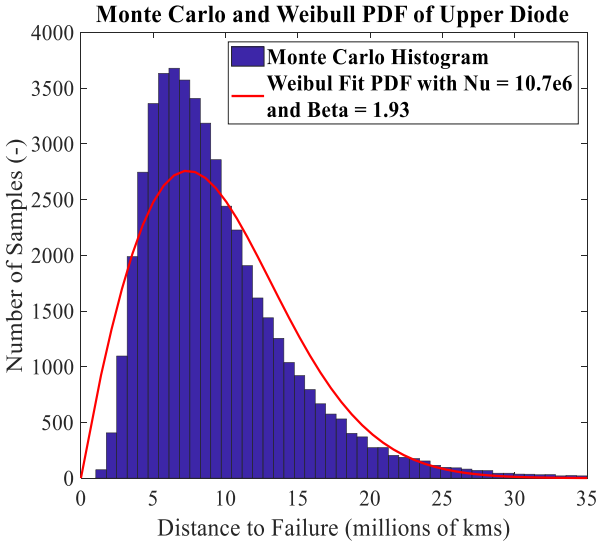
the upper and lower MOSFETs, the upper and lower diodes, and the DC-link capacitor, when the EV is subjected to the extra-urban mission profile.



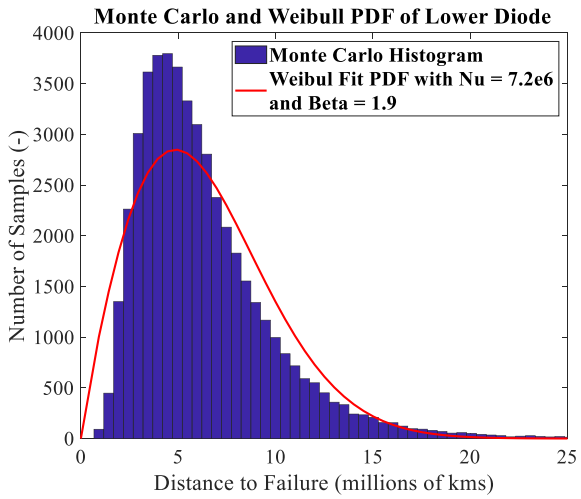
(a)



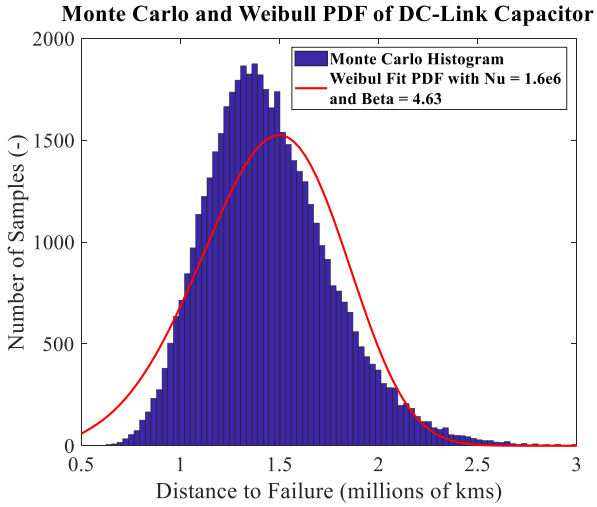
(b)



(c)



(d)



(e)

Fig. 25. A 100,000 sampling Monte Carlo method with Weibull's probability density function (PDF) for LESIT-based lifetime estimation with 10% parametric variation during ***extra-urban mission profile:*** (a) lifetime of Upper MOSFET, (b) lifetime of Lower MOSFET, (c) lifetime of Upper Diode, (d) lifetime of Lower Diode and (e) lifetime of DC-link Capacitor.

It can be seen from Fig. 25 (a)-(e) that the maximum population of the lower MOSFET $f_{LMOS}(t, \beta, \eta)$ fails after *1000 thousand* km of operation, while for the DC-link capacitor $f_{Cap}(t, \beta, \eta)$, it is *1500 thousand* km of operation. Therefore, it can be observed that based on LESIT model the lower MOSFET and the DC-link capacitor are the most failure-prone components in the IBC topology. The operational lifetime is around *10,000 thousand* km in upper MOSFET, lower and upper diodes, while most failure-prone components will fail way before that.

(b) Assessing the effect of TDDB on the system-level lifetime estimation

Based on the data provided by the device manufacturer [64], a Weibull approximation is made such that the probability density function (PDF) representing the device failure rate due to the TDDB corresponds to the OEM supplied values in the $R_{90\%}$, $R_{50\%}$ and $R_{10\%}$ percentile ranges; a normal distribution is assumed in the approximation, expressed as:

$$f(t,\beta,\eta) = \left(\frac{\beta}{\eta^{\beta}}\right).t^{(\beta-1)}.e^{-\left(\frac{t}{\eta}\right)^{\beta}} \quad for\ t \geq 0 \tag{30}$$

Where the shape parameter, $\beta = 76.6e^6$ and the scale parameter $\eta = 3.32$. The device-level lifetime determined from the Weibull distribution of the TDDB is combined as a series association to the device lifetime determined from the Weibull distribution of the LESIT model to obtain the overall device lifetime.

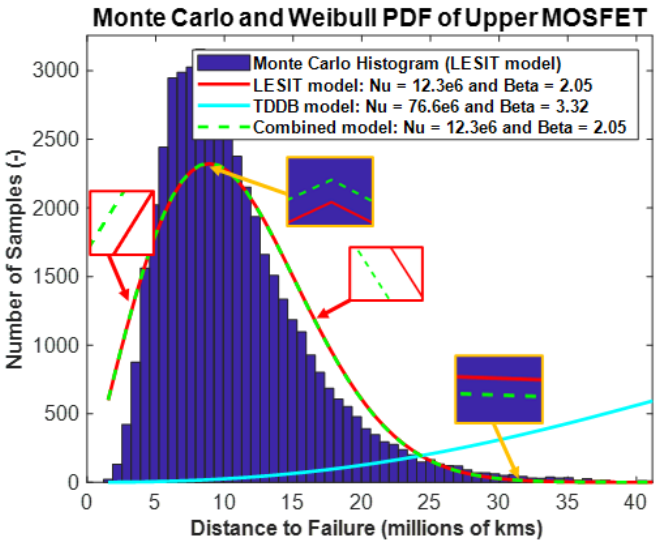


Fig. 26. A Monte Carlo method with Weibull's probability density function (PDF) for lifetime estimation of Upper MOSFET with the combined impact of 10% parametric variation + TDDB effect during extra-urban mission profile. A zoomed in version is shown to differentiate the PDF of the LESIT only and combined model.

The zoomed portions of Fig. 26 show slight changes in the Weibull distribution PDF, when the effects of TDDB are considered. It is noticed that the failure rate of the combined PDF *(LESIT+TDDB)* slightly leads to the failure rate of the LESIT only PDF. Thus, it can be concluded that the TDDB affects device lifetime at the component-level. Table 7 summarizes the device failure rate for the SiC MOSFETs when accounting the TDDB. It is found from Table 7 that, during the extra-urban mission, the highest mileage difference between the LESIT only and combined model is observed for the Upper SiC MOSFET, which is the least failure-prone component. In the combined model, reliability is around 4.3 thousand km lower for $R_{90\%}$ lifetime and around 21.2 thousand km lower for $R_{10\%}$ lifetime. In case of urban mission profile, the highest mileage difference is also found for Upper MOSFET, which is 8.7 thousand km less for $R_{90\%}$ lifetime and 47.4 thousand km less for $R_{10\%}$ lifetime. On the other hand, the most failure-prone component, which is the lower MOSFET, is the least affected by the TDDB due to the fact that the effect of the TDDB appears over the long term.

C. System-level lifetime formulation process

Once, the component level lifetime is determined, the next step is to calculate the lifetime of the entire IBC system. This is achieved by first establishing the failure association between the components via simulation. Failure association can be of two types, namely series failure association or parallel failure association. In a series failure association, a failure in any component will cause the entire system to fail. On the other hand, in a parallel association, all the components need to fail before the system fails, i.e., there is redundancy in the system. A special subset of parallel association is the k-out-of-n parallel association, where k number of components out of n parallel components need to fail in order to cause a system failure. Equations (31) to (33) express the calculation for the system lifetime from each of the individual component lifetime based on each types of failure associations.

Series failure association:

$$R(sys) = R_1.R_2.R_3 \ldots R_n \; for\; t \geq 0 \tag{31}$$

Parallel failure association:

$$1\text{-}R(sys) = (1-R_1).(1-R_2).\ldots.(1-R_n) \; for\; t \geq 0 \tag{32}$$

Where R_N is the n^{th} component in the system. k-out-of-n parallel failure association (32):

$$R(sys) = \sum_{l=k}^{n} \binom{n}{l} r(t)^l \left(1-r(t)\right)^{n-l} \tag{33}$$

Where *R(sys)* is the reliability of the component in the t^{th} time instant, n is the total number of parallel components in a system, and k is the minimum number of component failures that will cause a system failure. In k-out-of-n parallel associations, all parallel components are assumed to have similar reliability.

The simulation model of the IBC is used to determine the type of failure association between components when each of the components suffers "*Short-circuit*" or "*Open-circuit*" failure conditions. It is observed from the simulation that all component failures are in series association for short-circuit conditions; hence, there is no redundancy in the system. On the other hand, for the open circuit condition, the failure association for the lower MOSFET of a given phase, with the lower MOSFET of the other two phases, is in the 2-out-of-3 parallel association, so there is redundancy in the system for the lower MOSFET. The failures of upper and lower diodes and DC-link capacitor show series association, while upper MOSFET's failure has no impact on the system. Equations (34)-(36) describe the system lifetime reliability for the two failure scenarios.

For short circuit condition (no redundancy):

$$R(sys) = {R_{LMOS}}^3.{R_{LDio}}^3.{R_{UMOS}}^3.{R_{UDio}}^3.R_C \tag{34}$$

For open-circuit condition (redundancy):

$$R(sys) = {R_{LDio}}^3.{R_{UDio}}^3.R_C \sum_{l=2}^{3} \binom{3}{l} {R_{LMOS}}^l \left(1-{R_{LMOS}}^l\right)^{3-l} \tag{35}$$

$$= {R_{LDio}}^3.{R_{UDio}}^3.R_C(3.{R_{LMOS}}^2 - 2.{R_{LMOS}}^3) \tag{36}$$

Where R_{LMOS} is the reliability of the lower MOSFET, R_{UMOS} is the reliability of the upper MOSFET, R_{LDio} is the reliability of the lower Diode, R_{UDio} is the reliability of the upper Diode, and R_C is the reliability of the DC-link capacitor.

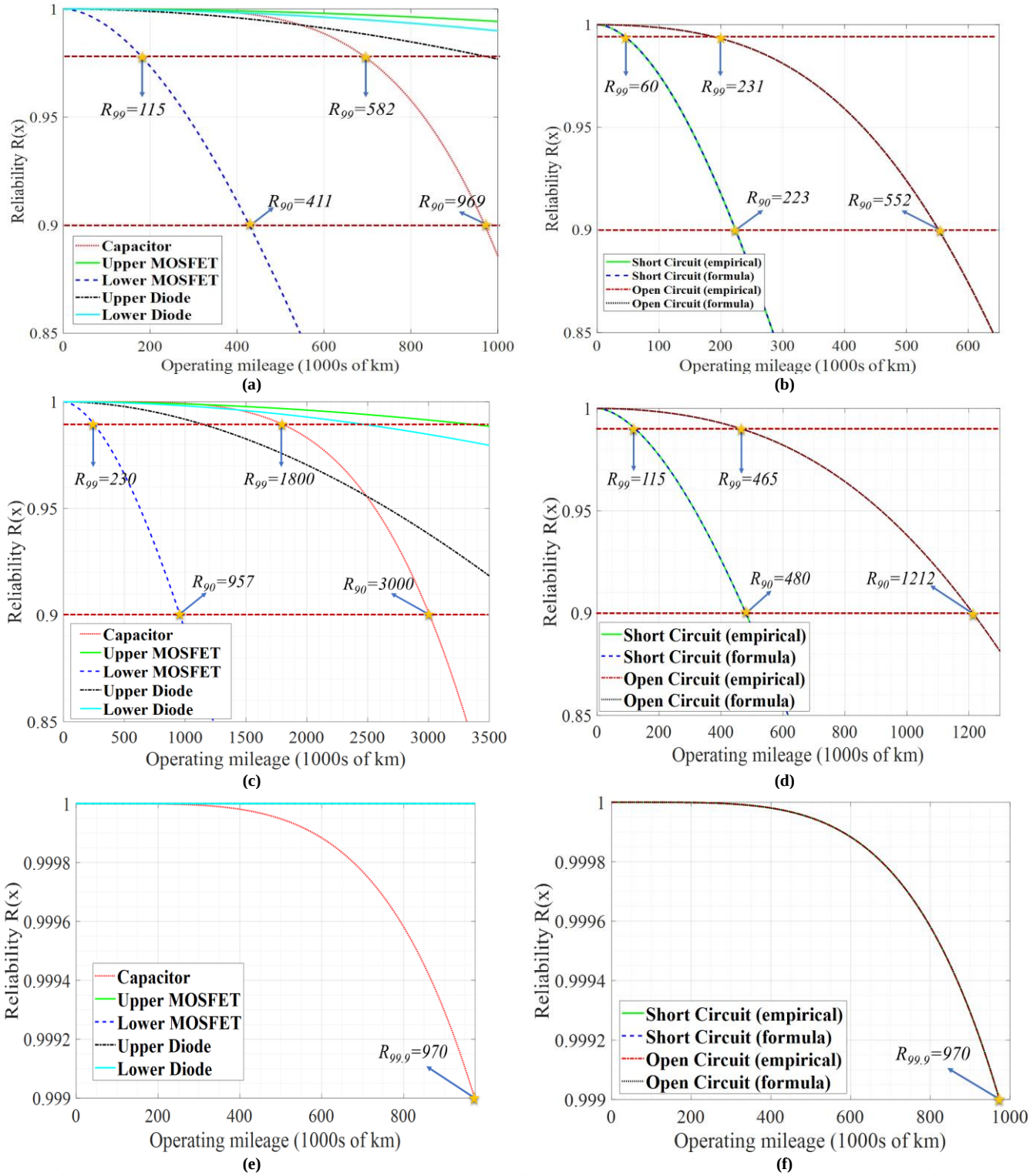


Fig. 27. Lifetime estimation results considering LESIT and TDDB parameters effect, respectively: ***Extra-Urban mission profile:*** (a) lifetime of Components, (b) lifetime of IBC System (with and without redundancy both for formula and empirical method), ***Urban mission profile:*** (c) lifetime of Components, (d) lifetime of IBC System (with and without redundancy both for formula and empirical method), and ***Continuous hill-climbing mission profile:*** (e) lifetime of Components, (f) lifetime of IBC System (with and without redundancy both for formula and empirical method).

D. System-level lifetime estimation of the IBC considering LESIT and TDDB parameters

The automotive OEMs commonly express component lifetime in terms of mileage (i.e., thousand kilometres) travelled, instead of years of service. The distance travelled in kilometres can be determined by multiplying the lifetime, expressed in hours, by the average speed, in km/hr, of the mission velocity profile. The lifetime of the individual components and the entire IBC system corresponding to separate mission profiles are depicted in Fig. 27 (a)-(e), where the TDDB impacts on SiC MOSFET modules are also considered.

Table 7. Effect of TDDB on Individual Component Reliability and on IBC System Reliability

Extra-Urban Mission	LESIT model lifetime in mileage (km)			Combined model Lifetime in mileage (km)			Difference in mileage (km)		
	$R_{90\%}$	$R_{50\%}$	$R_{10\%}$	$R_{90\%}$	$R_{50\%}$	$R_{10\%}$	$R_{90\%}$	$R_{50\%}$	$R_{10\%}$
Upper MOSFET	4109901	10285789	18455868	4105610	10274411	18434722	4291	11378	21146
Lower MOSFET	428262	1224038	2390284	428262	1224037	2390280	0	1	4
System-level reliability Short circuit (SC)	223800	629400	1163800	223800	629360	1163800	0	40	0
System-level reliability Open circuit (OC)	552100	1038200	1523460	552100	1038200	1523420	0	0	40
Urban Mission	LESIT model lifetime in mileage (km)			Combined model Lifetime in mileage (km)			Difference in milage (km)		
	$R_{90\%}$	$R_{50\%}$	$R_{10\%}$	$R_{90\%}$	$R_{50\%}$	$R_{10\%}$	$R_{90\%}$	$R_{50\%}$	$R_{10\%}$
Upper MOSFET	11017137	29287902	54612287	11008427	29263367	54564900	8710	24535	47387
Lower MOSFET	957040	2870757	5781251	957041	2870756	5781246	-1	1	5
System-level reliability Short circuit (SC)	480000	1423050	2801400	479960	1423050	2801365	40	0	35
System-level reliability Open circuit (OC)	1212650	2493400	3000000	1212605	2493400	3000000	45	0	0

The component-level and system-level lifetime of the IBC are expressed in R_x (i.e., R_{99}, R_{90} and $R_{99.9}$) and indicated in Fig. 27. Mainly, for automotive applications, the point of lifetime interest is R_{99}, reflecting a 99% reliability percentile.

As mentioned in the previous subsection, the most failure-prone component is the lower MOSFET; and the R_{99} of lower MOSFET is 115 and 230 thousand kilometres, respectively, for extra-urban and urban mission profiles. The worst-case lifetime of the IBC system, which takes place during the extra-urban mission profile without any redundancy, is 60 thousand kilometres for R_{99}. For the urban mission profile, the IBC's lifetime R_{99} is 115 thousand kilometres. However, in the open-circuit condition, the lower MOSFET shows 2-out-of-3 redundancy, and the failure of the upper MOSFET has no impact on the system.

Due to the aforementioned redundancy, the reliability percentile R_{99} of the IBC improves significantly, approximately 75%, compared to the short circuit condition. The target lifetime requirement of the OEM for the HV DC/DC converter of the EV is typically 300 thousand kilometres. The worst-case scenario of the IBC, which is the Extra-Urban mission profile without redundancy, is 18% component failure after 300 thousand kilometres travelled, and only 2% failure with redundancy. It can be noticed that the reliability value for the hill-climbing profile, for 300 thousand kilometres, is high at $R_{99.9}$, but this value has a low confidence since the hill climbing profile uses fewer number of samples for stress analysis.

In addition, Table 7 depicts that the effect on lifetime, due to TDDB, is negligible on the system level (maximum around 0.045 thousand km); this is due to the fact that the system-level lifetime is closely tied to the reliability of the most failure-prone components.

E. Lifetime estimation validation through empirical method

To ensure the validity of the lifetime estimation analysis, the system-level lifetime calculated from empirical data of individual component-level lifetime, using equations (36) and (35), is compared to analytical results calculated by combining the shape and scale parameter of the individual component Weibull distributions into one, before applying equation (29), as shown in equations (37) and (38). However, in order to simplify the overall equation, intermediate terms are defined first:

$$nb_{UMOS} = \eta_{UMOS}{}^{\beta_{UMOS}},\ nb_{LMOS} = \eta_{LMOS}{}^{\beta_{LMOS}},$$
$$nb_{UDio} = \eta_{UDio}{}^{\beta_{UDio}},\ nb_{LDio} = \eta_{LDio}{}^{\beta_{LDio}},\ nb_C = \eta_C{}^{\beta_C}$$

Short circuit condition:

$$DEN_{sc} = nb_{UMOS}.nb_{LMOS}.nb_{UDio}.nb_{LDio}.nb_C$$
$$num_{UMOS} = nb_C.nb_{LMOS}.nb_{UDio}.nb_{LDio}$$
$$num_{LMOS} = nb_{UMOS}.nb_C.nb_{UDio}.nb_{LDio}$$
$$num_{UDio} = nb_{UMOS}.nb_{LMOS}.nb_C.nb_{LDio}$$
$$num_{LDio} = nb_{UMOS}.nb_{LMOS}.nb_{UDio}.nb_C$$
$$num_C = nb_{UMOS}.nb_{LMOS}.nb_{UDio}.nb_{LDio}$$
$$NUM_{sc} = 3num_{UMOS}.t^{\beta_{UMOS}} + 3num_{LMOS}.t^{\beta_{LMOS}} + 3num_{UDio}.t^{\beta_{UDio}} + 3num_{LDio}.t^{\beta_{LDio}} + num_C.t^{\beta_C}$$
$$R(sys) = e^{-\frac{NUM_{sc}}{DEN_{sc}}}\ for\ t \geq 0 \quad (37)$$

Open circuit condition:

$$DEN_{oc} = nb_{LMOS}.nb_{UDio}.nb_{LDio}.nb_C$$
$$num_{LMOS} = nb_C.nb_{UDio}.nb_{LDio}$$
$$num_{UDio} = nb_{LMOS}.nb_C.nb_{LDio}$$
$$num_{LDio} = nb_{LMOS}.nb_{UDio}.nb_C$$
$$num_C = nb_{LMOS}.nb_{UDio}.nb_{LDio}$$
$$NUM_{oc1} = 2num_{LMOS}.t^{\beta_{LMOS}} + 3num_{UDio}.t^{\beta_{UDio}} + 3num_{LDio}.t^{\beta_{LDio}} + num_C.t^{\beta_C}$$
$$NUM_{oc2} = 3num_{LMOS}.t^{\beta_{LMOS}} + 3num_{UDio}.t^{\beta_{UDio}} + 3num_{LDio}.t^{\beta_{LDio}} + num_C.t^{\beta_C}$$
$$R(sys) = 3e^{-\frac{NUM_{oc1}}{DEN_{sc}}} - 2e^{-\frac{NUM_{oc2}}{DEN_{sc}}}\ for\ t \geq 0 \quad (38)$$

Where η is the scale parameter, β is the shape parameter, LMOS is the lower MOSFET, UMOS is the upper MOSFET, LDio is the lower Diode, UDio is the upper Diode, *C* is the DC-link capacitor, and '*t*' is the time duration. Fig. 27(b), (d) and (f) depict that there is approximately no difference (less than 10^{-4}) between the lifetime determined from the empirical data and the lifetime calculated analytically, thus validating the equations used for lifetime estimation.

VI. Conclusion

In this paper, the impact of real-life EV mission profiles on the PE converter lifetime, essentially an automotive HV DC/DC converter, has been investigated. For the first time, to the best knowledge of the authors, separate initial battery SoC windows have been utilised to conduct the lifetime estimation. The battery pack design has been validated with RT measurement using accurate mission profiles during the lifetime estimation. A high degree of correlation has been achieved in battery pack modelling (*i.e.,* a *minimal 94%* and a *maximum of 99%*) for all three profiles. Furthermore, in the IBC modelling peak *0.2%* MPE is obtained between model estimated efficiency and experimental measurement for *10%-100%* load changes for boost mode and buck mode operations, respectively.

The assessment showed a significant impact of the mission profiles on the lifetime of the converter system. Furthermore, it is noticed that for the IBC, redundancy improves the lifetime at *300 thousand* kilometres by *16%* in the extra-urban profile and by *4%* in the urban profile. However, the IBC is four times more reliable when the EV is driving using the urban profile compared to the extra-urban profile. This is caused as the extra-urban driving profile is characterized by frequent accelerations and decelerations, which cause higher electro-thermal stress in the semiconductor components, accelerating the wear-out failure. Moreover, it has been observed that mission-profile less than *500 sec* is not appropriate for the accurate system-level lifetime estimation of automotive PEC. In this paper, it has also been identified that the lower MOSFET and DC-link capacitor are the most failure-prone components in terms of reliability percentile *Rx*, which determine the lifetime performance of the IBC system. However, it is worth to mention that the SiC MOSFET-based HV DC/DC converter topology (IBC) using a dual-loop type-II k factor-based control technique has been satisfied the targeted lifetime requirements of the BEVs for both mission profiles. Additionally, the SiC MOSFET power modules are also affected by the TDDB, which causes a reliability issue over the long-term. Hence, the most failure prone components are less affected by the TDDB, while more reliable components experience higher effects due to the TDDB. The effect of TDDB on the system-level reliability of the IBC is less than even one thousand km for reliability percentile of R_{10}, with or without redundancy. The TDDB impact is negligible since the system reliability is similar to the corresponding one of the most failure-prone components. Thus, the IBC system, whether there is redundancy or not, do not last long enough under the given mission profiles, to experience the effects of TDDB.

Although lifetime for semiconductor-based PE systems has been investigated in the literature, this has been done mainly for systems incorporated inside stationary applications (i.e., solar and wind) and primarily relying on passive cooling. This paper has investigated the automotive PE systems that subjected to dynamic load profiles and incorporating active cooling strategies.

Furthermore, in this paper, an automotive PEC system has been evaluated through OEM-provided real-life mission profiles; thus, this paper overcomes the uncertainties generated due to the unavailability of real-life missions. In future research, the lifetime model of the IBC will be incorporated with a digital twin for reliability (*DT4R*) model to schedule predictive maintenance before a potential failure through accurate wear-out and degradation monitoring.

Appendix

The formulas that have been used in Kendall's rank correlation are expressed in equation (39)-(43).

$$\tau = \frac{(number\ of\ concordant\ pair) - (number\ of\ discordant\ pair)}{(Total\ number\ of\ parings)} \quad (39)$$

$$\tau = \frac{n_c - n_d}{n_0} \quad (40)$$

$$\tau = \frac{2K}{n(n-1)} \quad (41)$$

$$where\ K \sum_{i=1}^{n-1} \sum_{j=i+1}^{n} \xi^*\left(X_{a,i}, X_{a,j}, Y_{b,i}, Y_{b,j}\right) \quad (42)$$

$$\xi^*\left(X_{a,i}, X_{a,j}, Y_{b,i}, Y_{b,j}\right) = \begin{cases} 1 & \left(X_{a,i}, X_{a,j}\right)\left(Y_{b,i}, Y_{b,j}\right) > 0 \\ 0 & \left(X_{a,i}, X_{a,j}\right)\left(Y_{b,i}, Y_{b,j}\right) = 0 \\ -1 & \left(X_{a,i}, X_{a,j}\right)\left(Y_{b,i}, Y_{b,j}\right) < 0 \end{cases} \quad (43)$$

Where τ is the ordinal association between model data and measurement data sets, in this paper, the significance level for the Correlation test is considered 0.001.

The MPE equation is expressed in equation (44).

$$MPE = \frac{|(Measurement\ data - Model\ data)|}{Model\ data} \times 100\% \quad (44)$$

Acknowledgement

This project (HiFi-Elements) has received funding partially from the European Union's Horizon 2020 research and innovation program under Grant Agreement no. 769935. We also acknowledge Flanders Make for their support to this research group.

References

[1] "Global EV Outlook 2020," *Glob. EV Outlook 2020*, 2020.

[2] J. Van Mierlo *et al.*, "Beyond the State of the Art of Electric Vehicles: A Fact-Based Paper of the Current and Prospective Electric Vehicle Technologies," *World Electr. Veh. J.*, vol. 12, no. 1, p. 1-20, Feb. 2021.

[3] F. Blaabjerg, H. Wang, I. Vernica, B. Liu, and P. Davari, "Reliability of Power Electronic Systems for EV/HEV Applications," *Proc. IEEE*, pp. 1–17, 2021.

[4] F. H. Gandoman *et al.*, "Status and future perspectives of reliability assessment for electric vehicles," *Reliab. Eng. Syst. Saf.*, vol. 183, no. May 2018, pp. 1–16, 2019.

[5] K. Hu, Z. Liu, Y. Yang, F. Iannuzzo, and F. Blaabjerg, "Ensuring a Reliable Operation of Two-Level IGBT-Based Power Converters: A Review of Monitoring and Fault-Tolerant Approaches," *IEEE Access*, vol. 8, pp. 89988–90022, 2020.

[6] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, 2011.

[7] M. Chen, H. Wang, F. Blaabjerg, X. Wang, and D. Pan, "A Temperature-dependent Thermal Model of Silicon Carbide MOSFET Module for Long-term Reliability Assessment," *2018 IEEE 4th South. Power Electron. Conf. SPEC 2018*, pp. 1–7, 2018.

[8] S. Baba, A. Gieraltowski, M. Jasinski, F. Blaabjerg, A. S. Bahman, and M. Zelechowski, "Active Power Cycling Test Bench for SiC Power MOSFETs - Principles, Design, and Implementation," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2661–2675, 2021.

[9] S. Chakraborty *et al.*, "Reliability Assessment of a WBG-based Interleaved Bidirectional HV DC/DC Converter for Electric Vehicle Drivetrains," *2020 15th Int. Conf. Ecol. Veh. Renew. Energies, EVER 2020*, 2020.

[10] T. Ziemann, U. Grossner, and J. Neuenschwander, "Power Cycling of Commercial SiC MOSFETs," *2018 IEEE 6th Work. Wide Bandgap Power Devices Appl. WiPDA 2018*, pp. 24–31, 2018.

[11] X. Yang *et al.*, "Degradation Behavior and Defect Analysis for SiC

Power MOSFETs Based on Low-Frequency Noise Under Repetitive Power-Cycling Stress," in *IEEE Transactions on Electron Devices*, vol. 68, no. 2, pp. 666-671, Feb. 2021.

[12] F. Yang, E. Ugur, and B. Akin, "Design Methodology of DC Power Cycling Test Setup for SiC MOSFETs," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 4, pp. 4144–4159, 2020.

[13] S. Geraei and S. H. Aghdam, "Power cycling test bench for accelerated life testing for reliability assessment of SiC-MOSFET in extreme offshore environment," *arXiv*, no. 1, pp. 1–9, 2020.

[14] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectron. Reliab.*, vol. 42, no. 4–5, pp. 653–667, Apr. 2002.

[15] H. Luo, P. D. Reigosa, F. Iannuzzo, and F. Blaabjerg, "On-line solder layer degradation measurement for SiC-MOSFET modules under accelerated power cycling condition," *Microelectron. Reliab.*, vol. 88–90, no. February 2019, pp. 563–567, 2018.

[16] C. T. Yen *et al.*, "Oxide Breakdown Reliability of SiC MOSFET," in *2019 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, 2019, pp. 1–3.

[17] T. T. Nguyen, A. Ahmed, T. V. Thang, and J.-H. Park, "Gate Oxide Reliability Issues of SiC MOSFETs Under Short-Circuit Operation," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2445–2455, May 2015.

[18] M. N. Zulkifli, S. Abdullah, N. K. Othman, and A. Jalar, "Some thoughts on bondability and strength of gold wire bonding," *Gold Bull.*, vol. 45, no. 3, pp. 115–125, Sep. 2012.

[19] A. Volke and H. Michael, *IGBT Modules. Technologies, Driver and Application*. 2017.

[20] M. Thoben, F. Sauerland, K. Mainka, S. Edenharter, and L. Beaurenaut, "Lifetime modeling and simulation of power modules for hybrid electrical/electrical vehicles," *Microelectron. Reliab.*, vol. 54, no. 9–10, pp. 1806–1812, 2014.

[21] Z. Zhao, D. Zhou, P. Davari, J. Fang, and F. Blaabjerg, "Reliability Analysis of Capacitors in Voltage Regulator Modules with Consecutive Load Transients," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2481–2487, 2021.

[22] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters - An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, 2014.

[23] M. Brüll, A. Ayad, A. Greif, S. Rogge, and M. Töns, "Lifetime Analysis of Electronics and Power Electronic Components in Electric Vehicles," in *32 nd Electric Vehicle Symposium (EVS32)*, 2019, pp. 1–12.

[24] M. Bruell, P. Brockerhoff, F. Pfeilschifter, H. P. Feustel, and W. Hackmann, "Bidirectional charge and traction-system," *World Electr. Veh. J.*, vol. 8, no. 1, pp. 237–248, 2016.

[25] Morgan Stanley, "The Climate Opportunity of Auto 2.0: How Big Tech Drives Faster EV Adoption," last accessed on 10 Januray, 2021, https://www.morganstanley.com/ideas/ride-sharing-electric-vehicles-carbon-emissions.

[26] S. Chakraborty *et al.*, "Scalable Modelling Approach & Robust Hardware-in-the-Loop Testing of an Optimized Interleaved Bidirectional HV DC/DC Converter for Electric Vehicle Drivetrains," *IEEE Access*, vol. 8, pp. 115515–115536, 2020.

[27] K. Etzold *et al.*, "Hardware-in-the-Loop Testing of Electric Traction Drives with an Efficiency Optimized DC-DC Converter Control," *SAE Tech. Pap.*, vol. 2020-April, no. April, pp. 1–10, 2020.

[28] Y. Song and B. Wang, "Quantitative evaluation for reliability of hybrid electric vehicle powertrain," *Int. Conf. Power Eng. Energy Electr. Drives*, vol. 5, pp. 1404–1409, 2013.

[29] V. Mulpuri, M. Haque, M. N. Shaheed, and S. Choi, "Multistate Markov Analysis in Reliability Evaluation and Life Time Extension of DC-DC Power Converter for Electric Vehicle Applications Vamsi," *2018 IEEE Transp. Electrif. Conf. Expo*, pp. 280–285, 2018.

[30] A. H. Ranjbar and B. Fahimi, "Helpful hints to enhance reliability of DC-DC converters in hybrid electric vehicle applications," *2010 IEEE Veh. Power Propuls. Conf. VPPC 2010*, 2010.

[31] M. Mürken and P. Gratzfeld, "Reliability comparison of bidirectional automotive DC/DC converters," *IEEE Veh. Technol. Conf.*, vol. 2017-Septe, pp. 1–7, 2018.

[32] Y. Song and B. Wang, "Evaluation methodology and control strategies for improving reliability of HEV power electronic system," *IEEE Trans. Veh. Technol.*, vol. 63, no. 8, pp. 3661–3676, 2014.

[33] S. Peyghami, P. Davari, and F. Blaabjerg, "System-Level Reliability-Oriented Power Sharing Strategy for DC Power Systems," *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 4865–4875, 2019.

[34] N. Omar *et al.*, "Lithium iron phosphate based battery – Assessment of the aging parameters and development of cycle life model," *Appl. Energy*, vol. 113, pp. 1575–1585, Jan. 2014.

[35] I. Mudawar, D. Bharathan, K. Kelly, and S. Narumanchi, "Two-Phase Spray Cooling of Hybrid Vehicle Electronics," *IEEE Trans. Components Packag. Technol.*, vol. 32, no. 2, pp. 501–512, Jun. 2009.

[36] U. Scheuermann, "Reliability challenges of automotive power electronics," *Microelectron. Reliab.*, vol. 49, no. 9–11, pp. 1319–1325, Sep. 2009.

[37] X. Perpina, X. Jorda, M. Vellvehi, J. Rebollo, and M. Mermet-Guyennet, "Long-Term Reliability of Railway Power Inverters Cooled by Heat-Pipe-Based Systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2662–2672, Jul. 2011.

[38] A. Najmabadi, K. Humphries, and B. Boulet, "Implementation of a bidirectional DC-DC in electric powertrains for drive cycles used by medium duty delivery trucks," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 1338–1345.

[39] A. Najmabadi, K. Humphries, and B. Boulet, "Application of a bidirectional DC-DC in an electric powertrain for medium duty delivery trucks," in *2015 IEEE International Electric Machines & Drives Conference (IEMDC)*, 2015, pp. 866–871.

[40] A. A. E. Abdallh and M. Witters, "Optimal Control and Design of Hybrid Electric Vehicles Including Bi-Directional DC-DC Converters," in *2017 IEEE Vehicle Power and Propulsion Conference (VPPC)*, 2017, pp. 1–5.

[41] S. Chakraborty, H. Vu, M. M. Hasan, D. Tran, M. El Baghdadi, and O. Hegazy, "DC-DC Converter Topologies for Electric Vehicles, Plug-in Hybrid Electric Vehicles and Fast Charging Stations: State of the Art and Future Trends," *Energies*, vol. 12, no. 8, p. 1569, Apr. 2019.

[42] D. Tran, S. Chakraborty, Y. Lan, J. Van Mierlo, and O. Hegazy, "Optimized Multiport DC/DC Converter for Vehicle Drivetrains: Topology and Design Optimization," *Appl. Sci.*, no. 8: 1351, *pp. 1-17*, 2018.

[43] E. Nazeraj, O. Hegazy, and J. Van Mierlo, "Control Design , Analysis and Comparative study of Different Control Strategies of a Bidirectional DC / DC Multiport Converter for Electric Vehicles," *Evs30*, pp. 1–14, 2017.

[44] O. Hegazy, R. Barrero, J. Van Mierlo, P. Lataire, N. Omar, and T. Coosemans, "An Advanced Power Electronics Interface for Electric Vehicles Applications," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5508–5521, Dec. 2013.

[45] S. Chakraborty, D. D. Tran, J. Van Mierlo, and O. Hegazy, "Generalized Small-Signal Averaged Switch Model Analysis of a WBG-based Interleaved DC/DC Buck Converter for Electric Vehicle Drivetrains," *2020 22nd Eur. Conf. Power Electron. Appl. EPE 2020 ECCE Eur.*, pp. 1–8, 2020.

[46] J. W. Kolar, "A General Scheme for Calculating Switching- and Conduction-Losses of Power Semiconductors in Numerical Circuit Simulations of Power Electronic Systems," in *International Power Electronics Conference (IPEC05), Niigata,Japan, April.*, 2005, pp. 4–8.

[47] N. C. Sintamarean, F. Blaabjerg, H. Wang, and Y. Yang, "Real field mission profile oriented design of a SiC-Based PV-inverter application," *IEEE Trans. Ind. Appl.*, vol. 50, no. 6, pp. 4082–4089, 2014.

[48] W. Jouha, A. El Oualkadi, P. Dherbécourt, M. Masmoudi, and E. Joubert, "In-depth analysis of the static behaviour of a SiC MOSFET and of its associated parameters using both compact modelling and physical simulation," *IET Circuits, Devices Syst.*, vol. 14, no. 2, pp. 222–228, Mar. 2020.

[49] W. Jouha, A. El Oualkadi, P. Dherbecourt, E. Joubert, and M. Masmoudi, "Silicon Carbide Power MOSFET Model: An Accurate Parameter Extraction Method Based on the Levenberg–Marquardt Algorithm," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9130–9133, Nov. 2018.

[50] B. W. Nelson *et al.*, "Computational Efficiency Analysis of SiC MOSFET Models in SPICE: Static Behavior," *IEEE Open J. Power Electron.*, vol. 1, pp. 499–512, 2020.

[51] B. W. Nelson *et al.*, "Computational Efficiency Analysis of SiC MOSFET Models in SPICE: Dynamic Behavior," *IEEE Open J. Power Electron.*, vol. 2, pp. 106–123, 2021.

[52] Y. Zhou, "SPICE Modeling of SiC MOSFET Considering Interface-

Trap Influence," *CPSS Trans. Power Electron. Appl.*, vol. 3, no. 1, pp. 56–64, Mar. 2018.
[53] B. Duan, X. Yang, J. Lv, and Y. Yang, "Novel SiC/Si Heterojunction Power MOSFET With Breakdown Point Transfer Terminal Technology by TCAD Simulation Study," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3388–3393, Aug. 2018.
[54] B. Duan, S. Xue, X. Huang, and Y. Yang, "Novel Si/SiC Heterojunction Lateral Double-Diffused Metal Oxide Semiconductor With SIPOS Field Plate by Simulation Study," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 114–120, 2021.
[55] L. Chen, X. Yao, and S. Cen, "Predictions of elastic property on 2.5D C/SiC composites based on numerical modeling and semi-analytical method," *Compos. Part B Eng.*, vol. 74, pp. 53–65, Jun. 2015.
[56] Datasheet Metglas Inc., "Inductor Cores, Powerlite Technical Bulletin, PLC09302008.," 2008.
[57] Datasheet(CDE Cornell Dubilier), "DC Link Capacitors Type 947C Polypropylene , High Current , High Capacitance for Inverter Applications," 2018.
[58] A. Wintrich, N. Ulrich, T. Werner, and T. Reimann, *Application Manual Power Semiconductors*. 2015.
[59] A. Anurag, Y. Yang, and F. Blaabjerg, "Reliability analysis of single-phase PV inverters with reactive power injection at night considering mission profiles," *2015 IEEE Energy Convers. Congr. Expo. ECCE 2015*, pp. 2132–2139, 2015.
[60] W. Huai *et al.*, "Transitioning to physics-of-failure as a reliability driver in power electronics," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 2, no. 1, pp. 97–114, 2014.
[61] D. D. Tran *et al.*, "Multi-fidelity Electro-thermal optimization of Multiport Converter employing SiC MOSFET and Indirect Liquid Cooling," in *2019 Fourteenth International Conference on Ecological Vehicles and Renewable Energies (EVER)*, 2019, pp. 1–7.
[62] J. S. Suehle and S. Member, "Ultrathin Gate Oxide Reliability : Physical Models ," *IEEE Trans. Electron Devices*, vol. 49, no. 6, pp. 958–971, 2002.
[63] A. Agarwal, H. Fatima, S. Haney, and S.-H. Ryu, "A New Degradation Mechanism in High-Voltage SiC Power MOSFETs," *IEEE Electron Device Lett.*, vol. 28, no. 7, pp. 587–589, Jul. 2007.
[64] G. Moxey, "A Designers Guide to Silicon Carbide Power," Seminar on *Wolfspeed driving SiC long term adoption through reliability and capacity*, November, pp. 1–22, 2020.
[65] A. Sangwongwanich, Y. Yang, D. Sera, and F. Blaabjerg, "Lifetime Evaluation of Grid-Connected PV Inverters Considering Panel Degradation Rates and Installation Sites," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1125–1236, 2018.
[66] P. Tu, S. Yang, and P. Wang, "Reliability and cost-based redundancy design for modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2333–2342, 2019.
[67] M. Sandelic, A. Sangwongwanich, and F. Blaabjerg, "Reliability evaluation of PV systems with integrated battery energy storage systems: DC-coupled and AC-coupled configurations," *Electron.*, vol. 8, no. 9, 2019.
[68] J. He, A. Sangwongwanich, Y. Yang, and F. Iannuzzo, "Lifetime Evaluation of Three-Level Inverters for 1500-V Photovoltaic Systems," *IEEE J. Emerg. Sel. Top. Power Electron.*, pp. 1–1, 2020.

Sajib Chakraborty (S'13-M' 16) was born in Chittagong, Bangladesh. He received the B.Sc. and M.Sc. degrees (Hons.) in electrical and electronic engineering from Independent University, Bangladesh, in 2013 and 2016, respectively. He was a lecturer with Independent University, Bangladesh from 2017 to 2018.

He is currently a Ph.D. Researcher with the EPOWERS-Efficient Power Electronics, Powertrain and Energy Solutions-Research Group, MOBI research centre, Vrije Universiteit Brussel. His research interests include accurate and scalable modelling of power electronics converters, physics of failure-based reliability analysis of the automotive power converters, digital twin architecture design of the PE converters, EV modelling and component selection optimization, and renewable energy technology. He is a topic editor of Energies and member of EPE.

Mohammed Mahedi Hasan received his M.Sc. in Mechatronics Engineering from the American University of Sharjah, Sharjah, United Arab Emirates, in 2006, and his B.Sc. in Electrical Engineering from the Georgia Institute of Technology, Georgia, United States of America, in 2002. He worked as an Electronics Engineer at the Research & Development Centre, UAE Armed Forces, between 2007 and 2012, and between 2014 and 2018, he worked as a Lecturer in private universities in Banglaesh.

Since October 2018, he is a Ph.D. candidate with the EPOWERS- Efficient Power Electronics, Powertrain and Energy Solutions- Research Group, MOBI research centre, Vrije Universiteit Brussel. He is currently working on the ASSURED-project – Fast Charging Systems (up to 600kW) for Busses based on WBG (SiC) technology. His research interests include drivetrain modelling, optimization, energy management, and statistical evaluation for reliability assessment.

McGahan Paul is a technical lead for Battery Systems Computer-Aided Engineering (CAE) at Ricardo. His expertise is in process modelling, advanced control design and estimation, particularly for xEV applications. Paul has over a decade of industrial experience. He joined Ricardo in 2018. Prior to joining Ricardo, Paul worked for Siemens as an application engineer and, more recently, for Honeywell as a Senior Research Engineer in the Process Control and Optimization R&D group. He holds a BE in mechanical engineering and an MSc in Instrumentation and Control Engineering from University College Dublin and Czech Technical University in Prague, respectively.

During his career, Paul has been involved in a range of projects, including Virtual Battery Design Toolchain development, Battery Management System development (algorithmic and hardware), Advanced control design for heat pumps, Advanced thermal management of hybrid and electric vehicles and Hybrid powertrain optimal control design.

Dai-Duong Tran (Member IEEE) obtained his Ph.D. from the Vrije Universiteit Brussel, Belgium in January 2021. Duong also received the M.Sc. degree in electrical engineering from Soongsil University, Seoul, Republic of Korea, in 2016 and a B.Sc. degree in electrical engineering from the Hanoi University of Science and Technology, Hanoi, Vietnam, in 2011.

Currently, he works as a postdoctoral researcher and a project manager at MOBI, the group of Efficient Power electronics, powertrain and energy solutions (EPOWERS). He is involved in different European and national projects, focusing on multidisciplinary codesign optimization framework, wideband gap-based power electronics converters (multiport converter, GaN/SiC inverter, Z-source inverter, offboard/ onboard charger, active front end), optimization of powertrain system for plug-in hybrid electric vehicles, integrated energy management strategies.

Thomas Geury holds a master's degree in electrical engineering, obtained at the Université Libre de Bruxelles (ULB) in 2012. He then obtained his PhD degree in Engineering Sciences and Technology in 2016, in joint supervision between the ULB (BEAMS Electrical Energy research centre) and the University of Lisbon (ULisbon), in the INESD-ID Power Electronics and Power Quality Group, with a FRIA grant. He also stayed for a few months at the University of Nottingham. His work focused on a new PV converter topology that uses a Matrix Converter to solve Power Quality issues on the distribution grid.

Thomas is now working as a postdoctoral researcher at MOBI in the field of power electronics and energy management systems. His activities involve research and management of EU and national research projects on power electronics, electric and (plug-in) hybrid vehicles, control systems, power management strategies, renewable energy and storage systems as well as simulation and modelling.

Pooya Davari (S'11–M'13-SM'19) received the B.Sc. and M.Sc. degrees in electronic engineering from University of Mazandaran (Noushirvani), Iran, in 2004 and 2008, respectively, and the Ph.D. degree in power electronics from QUT, Australia, in 2013. From 2005 to 2010, he was involved in several electronics and power electronics projects as a Development Engineer. From 2013 to 2014, he was with QUT, as a Lecturer. He joined Aalborg University, in 2014, as a Postdoc, where he is currently an Associate Professor.

He has been focusing on EMI, power quality and harmonic mitigation analysis and control in power electronic systems. He has published more than 160 technical papers. Dr. Davari served as a Guest Associate Editor of IET journal of Power Electronics, IEEE Access Journal, Journal of Electronics and Journal of Applied Sciences. He is an Associate Editor of Journal of Power Electronics, Associate Editor of IET Electronics, Power Electronic Devices and Systems, Editorial board member of Journal of Applied Sciences and Journal of Magnetics. He is member of the International Scientific Committee (ISC) of EPE (ECCE Europe) and a member of Joint Working Group six and Working Group eight at the IEC standardization TC77A. Dr. Davari is the recipient of a research grant from the Danish Council of Independent Research (DFF-FTP) in 2016, and 2020 IEEE EMC Society Young Professional Award for his contribution to EMI and Harmonic Mitigation and Modeling in Power Electronic Applications. He is currently Editor-in-Chief of Circuit World Journal. He is founder and chair of IEEE EMC SOCIETY CHAPTER DENMARK.

Frede Blaabjerg (S'86–M'88–SM'97–F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia.

His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 600 journal papers in the fields of power electronics and its applications. He is the co-author of four monographs and editor of ten books in power electronics and its applications.

He has received 33 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014, the Global Energy Prize in 2019 and the 2020 IEEE Edison Medal. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2019-2020 he served as a President of IEEE Power Electronics Society. He has been Vice-President of the Danish Academy of Technical Sciences. He is nominated in 2014-2020 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.

Mohamed El Baghdadi (Member IEEE) holds a master's (Electromechanical Engineering) and doctor's degree in Engineering Sciences, obtained at the Vrije Universiteit Brussel, Belgium. After obtaining his M.Sc. degree (2009), his research focused on control engineering in the steel manufacturing's hot-strip rolling process. From 2011 his research was focused on electric and hybrid vehicles, drivetrain modeling & testing and wireless charging systems, while contributing to numerous national and European research projects in these fields and working as an academic teaching assistant. Since 2018, he works as a post-doctoral researcher in the field of power electronics, electric machines and (hybrid) electric vehicle powertrains at VUB's MOBI research centre, where he currently leads the vehicle powertrain team.

His activities include research and management of national and international projects in the domains of power electronics, electric machines, electric and hybrid vehicle powertrains and (wireless) charging. His main research interests are power & energy management strategies and control, design & optimization, (digital twin) simulation and system testing. He is also involved in teaching electrical engineering courses. He is an active member of EPE association.

Omar Hegazy (Member IEEE) received the B.Sc. (with honors) and M.Sc. degrees in Electrical Engineering, Helwan University, Cairo, Egypt. He obtained his Ph.D. degree in July 2012 (with greatest distinction) from the Dept. of Electrical Machines and Energy Technology (ETEC), Vrije Universiteit Brussel (VUB), Belgium.

He is the head of EPOWERS- Efficient Power Electronics, Powertrain and Energy Solutions- Research Group (Power Electronics Innovation Lab (PEIL), Powertrain Innovation Lab (PIL) & Joint Smart Charging Lab (JSCL)) at ETEC Dept., and at MOBI Research Centre, where he coordinates the research activities in this field in several national projects (e.g. via Flanders Make, VLAIO (ex. IWT), Innoviris, Flux50, etc.) and in European projects (e.g. SAFEDRIVE, UNPLUGGED, ELIPTIC, ORCA, ASSURED, HiFi-Elements, GHOST, HiPERFORM, ACHILES, LONGRUN, eCharge4drivers, iSTORMY, URBANIZED, HiEFFICIENT,etc.). He is also the manager of MOBI Core-Lab at Flanders Make organization. He is the author of more than 150 scientific publications and two patent applications. Furthermore, he is a member of EGVIA, EARPA, EPE and IEC standards.

His fields of interest include power electronics, electrical machines, electric and (plug-in) hybrid electric vehicles, Digital Twins (DT) & reliability, charging infrastructure, power/energy management strategies, battery management systems (BMS), V2X systems, optimization techniques and Smart DC grid with renewable energy.